A single event upset hardened flip-flop design utilizing layout technique

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A R T I C L E   I N F O

Keywords:
Quatro
Layout
Charge sharing
SEU

A B S T R A C T

A novel Quatro-based flip-flop design with low penalty was proposed. By utilizing layout technique, SEU hardness was achieved in this design because of charge sharing between the introduced PMOS transistors. Both the proposed design and the reference flip-flop were fabricated in a 65 nm standard CMOS technology. The pulsed laser experiment results demonstrate that the new design has a larger upset threshold and lower SEU error rate compared with the reference. The area and delay penalties are not significant, i.e., 13% and 37%, respectively.

1. Introduction

Single Event Effects (SEE) in Integrated Circuit (IC) may change the state of the system and result in soft errors [1]. In a combinational logic circuit, the factors of logic masking, electrical masking and latching-window masking can reduce soft error rate by preventing Single Event Transients (SETs) from propagating to the circuit outputs. However, in a sequential logic circuit, unhardened sequential elements, such as flip-flops, do not show such masking effects to Single Event Upsets (SEUs) [2].

There are two mechanisms that would likely generate SEUs in a flip-flop [3]: (1) the sensitive region of semiconductor devices inside a flip-flop is struck by a high energy particle, while the flip-flop is in the hold state; (2) an SET generated from its upstream circuit is captured by a flip-flop within the setup and hold time. Because the latter type of SEUs mainly depends on circuit speed, the majority of SEU hardening techniques are focused on mitigating the former type of SEUs.

In general, there are SEU mitigation techniques at different levels [4]. System-level hardening technologies, such as Error Correction Coding (ECC) and Triple Modular Redundancy (TMR), are widely used [5–7]. ECC is able to detect soft errors as they occur and correct them afterwards. In this technique, information and time redundancy are utilized to achieve the SEU hardness, which could result in observable delay penalties in the system. For TMR technique, each latch in the circuit is triplicated to prevent the propagation of soft errors. Although this approach improves SEU resilience effectively, it could introduce high area and power overhead.

Therefore, circuit-level technologies to mitigate SEU have drawn great research attention. One typical technique is adding either resistance or capacitance to the feedback path in order to increase node capacitance [8]. As the critical charge is proportional to node capacitance, this approach is able to increase critical charge of sensitive nodes and improve the SEU immunity of flip-flops. Radiation Hardening by Design (RHBD) can be used to mitigate soft errors by modifying circuit structure. The Dual Interlocked Storage Cell (DICE) [9] and 10 T-Quatro cell [10] are two typical novel latch designs based on the original 6 T memory cell. Although these structures show higher immunity to single node upset, they are still susceptible to multiple node upsets caused by charge sharing [11].

Charge sharing gets mitigated by using SOI technology [12]. This is widely used in silicon devices for charge collection mitigation and it has lower upset cross section compared with conventional CMOS bulk technology. As discussed, the original Quatro is not totally immune to single node upset during the hold state [13]. Therefore, a stacked Quatro was implemented in a commercial 28 nm CMOS fully-depleted SOI technology and presented superior SEU tolerance compared with the original Quatro [14].

However, this structure does not work in bulk technologies. Charge sharing is getting even worse, as the development of IC fabrication technology moves forward. Node capacitance and device spacing in...
2. Proposed design

2.1. Reference circuit and layout design

Fig. 1 shows the structure of the reference flip-flop design composed of two original Quatro latches. As can be seen, for a single Quatro latch, it has four storage nodes, two of which store the same value and the other two store the complement value.

The layout diagrams of the reference Quatro flip-flop are shown in Fig. 2, where the blue area is poly gate, the green area is active region, and the yellow area is N well.

For stable write and read operations in the Quatro latch, transistors need to be properly sized [10]. In our work, the external transistor ratio, e.g., \( W_{P4}/L_{P4} \)/(\( W_{N4}/L_{N4} \)), and internal transistor ratio, e.g., \( W_{P5}/L_{P5} \)/(\( W_{N5}/L_{N5} \)), are set as 0.4 and 0.6, respectively. This also guarantees that the Quatro design is immune to single node upset when node A or D is struck.

As discussed, a single ion hit may cause multiple node upsets caused by charge sharing between adjacent devices [16]. Quatro design is sensitive to multiple node upsets, especially when the two nodes holding the same logic value are struck at the same time. Therefore, for the master latch, P4 should be placed further from P6 in the layout, and P5 should be placed further from P7. Similarly, N4 and N6 as well as N5 and N7 should also be placed further from each other. This design rule has also been applied to the slave latch, as can be seen in Fig. 2.

Although Quatro design's immunity to multiple node upsets can be improved through layout design, it is still susceptible to single node upset when the internal node holding logic 0 is hit.

2.2. Proposed circuit and layout design

Our proposed flip-flop design is shown in Fig. 3. The storage cell is based on the original design and it also consists of 4 storage nodes. However, two more PMOS transistors are introduced compared with the reference latch. Take the master latch as an example, P5B is placed between the drain nodes of P5A and N5, while P6B is between the drain nodes of P6A and N6. Besides, the gates of P5B and P6B are connected to nodes A and D, respectively.

In this design, the SEU resilience is improved by utilizing layout technique. Fig. 4 illustrates the layout diagram of the proposed flip-flop. As can be seen, its layout is designed based on the reference Quatro layout structure.

For the master latch, P4 is placed away from P6A, and P5A is placed away from P7. Similarly, N4 is placed away from N6, and N5 is placed away from N7. What's more, the additional PMOS transistor P5B is placed adjacent to P6B and separated from P7. P6B is placed away from P4 in the layout. It is also noted that P5A is equally sized as P5B and twice as large as P5 in the reference master latch. It is the same thing for P6A and P6B. The transistors of the slave latch are set with the same layout design rule as the master latch.

2.3. Operating principles

By putting the two additional PMOS transistors of each latch adjacent in the layout, if one of them is struck by a single ion, it would affect the other transistor at the same time because of charge sharing and generate a transient at both nodes B and C. As a result, the two transistors would cancel out and the voltages at nodes B and C are able to recover after a time period. Therefore, the latch remains storing the correct logic values.

Suppose the logic values of the four storage nodes A, B, C, and D are 1, 0, 1 and 0 during the hold state, respectively. When P5B is struck by a single ion, the data of node B would flip from 0 to 1; and in the meantime, the voltage of node C will go up as well because of charge sharing between P5B and P6B. As a result, node B is capable of recovering; and the output nodes remain holding the correct values.

It is worth noting that charge sharing efficiency affects SEU hardening ability. Assume that the deposited charge at P5B of an ion is \( Q(P5B) \); the charge collected by P6B through charge sharing is \( Q(P6B) \); and \( Q(P6B)/Q(P5B) \) is defined as charge sharing efficiency.

The minimum charge sharing efficiency required not to upset the cell is plotted in Fig. 5 as a solid curve. The shaded area below this curve is the region of upset. For example, if 300 fC is deposited at P5B, charge sharing efficiency of 0.4 would make the latch upset. However, if the efficiency is as high as 1, the latch is immune to approximately 380 fC or even higher deposited at P5B.

Fig. 5 clearly shows that higher charge sharing results in higher SEU resilience. Therefore, in order to improve the charge sharing efficiency, P5B and P6B are placed much closer than the traditional way in the layout design. Therefore, this flip-flop design is believed to have superior SEU resilience compared with the reference Quatro design when any internal node is hit.

2.4. Overhead evaluation

Compared with the original Quatro flip-flop structure, the proposed design introduces 4 extra transistors and therefore slight penalty in area.

![Fig. 1. A reference flip-flop structure composed of two Quatro latches.](image)
and delay. The comparison is listed in Table 1.

The layout area of the Quatro flip-flop is 11.76 μm², and that of the proposed flip-flop is 13.32 μm². Then, the increase in layout area is ~13%. Although the additional PMOS transistors improve the SEU tolerance in the proposed design, they also increase delay time for propagation by ~37%. Besides, power consumption for the proposed design is almost the same as that for the Quatro design.

3. Simulation results

In our work, we simulate the current pulse introduced by a single ion hit by utilizing the double exponential current source model and its expression is presented in Eq. (1) [17].

\[ I(t) = I_0 \left( e^{-t/t_\alpha} - e^{-t/t_\beta} \right) \]

where \( I_0 \) is the maximum current, \( t_\alpha \) is the collection time constant of the junction, and \( t_\beta \) is the ion track establishment time constant. Assume \( Q \) be the amount of deposited charge and it can be expressed as \( I_0 s (t_\alpha - t_\beta) \).

In this paper, \( t_\alpha \) and \( t_\beta \) are set as 50 ps and 1 ns, respectively; and the simulation waveform of the injected current is shown in Fig. 6. For the sake of simplicity, all striking simulations are performed only for the master latch.

As the master latch of the original Quatro is symmetrical, suppose that the logic values of nodes A, B, C and D are 1, 0, 1 and 0 in the hold state, respectively. As discussed, Quatro is much more sensitive when node B is hit than any other storage node is hit. When node B is struck, the proposed design's SEU performance has been simulated to compare with the reference Quatro latch.

In the original Quatro latch, node B will flip from 0 to 1 when P5 is hit by injecting a charge as low as 112.1 fC, as shown in Fig. 7. As a result, the output nodes A and D will hold the incorrect values and will

<table>
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<td>1</td>
<td>1</td>
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<tr>
<td>Proposed design</td>
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Fig. 2. Layout diagram of the reference flip-flop; the blue area is poly gate, the green area is active region, and the yellow area is N well. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Fig. 3. The proposed flip-flop structure composed of two hardened latches.

Fig. 4. Layout diagram of the proposed flip-flop; the blue area is poly gate, the green area is active region, and the yellow area is N well. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Fig. 5. The minimum charge sharing efficiency required not to upset the cell for different charge deposited at P5B.
Fig. 6. The simulation waveform of injected current with $\tau_\beta$ of 50 ps and $\tau_\alpha$ of 1 ns.

Fig. 7. The simulation waveforms of all storage nodes in the Quatro latch when striking P5 by injecting 112.1 fC in the condition that A and C are 1, B and D are 0.

Fig. 8. The simulation waveforms of all storage nodes in the proposed latch when striking both P5B and P6B by injecting 632 fC in total in the condition that A and C are 1, B and D are 0.
However, the proposed design shows better SEU hardness than the reference one when the internal node holding logic 0 is hit. This is explained and simulated as follows. Likewise, we assume the logic values of nodes A, B, C and D in the master latch are 1, 0, 1 and 0, respectively.

When P5B is struck, P6B will be affected as well because of charge sharing between the two adjacent devices. The positive transient will flip node B; and in the meantime, it causes a build-up of the voltage at node C. As P5B and P6B are stacked near each other in the layout to maximize charge sharing, we assume the efficiency is 1 for our simulations. Therefore, P5B and P6B are struck at the same time by injecting two identical positive transients. The simulation waveforms are displayed in Fig. 8. As can be seen, the storage nodes are capable of recovering after a period of ~0.6 ns, when the maximum charge injected at both P5B and P6B is 632 fC in total. Therefore, it is obvious that the critical charge of the proposed design is much higher than that of the original Quatro latch (i.e., 112.1 fC) when P5 is struck. Please note due to the limitation of double exponential current source model, the critical charge is supposed to be much higher than the maximum charge [18].

Besides, when P5A is hit, the voltage of its drain node will increase. However, the state of P5B will not be affected because node A remains storing logic 1. As a result, the output will not flip. Therefore, the SEU hardness is increased in this proposed design through layout designing.

4. Test chip and system design

4.1. Test chip design

As illustrated in Fig. 9, 4000 proposed flip-flops and 4000 Quatro flip-flops are connected in two shift registers, each of which has a data input, a data output and two clock signal inputs. The area for the proposed flip-flop and the reference flip-flop is 13.32 μm × 2.6 μm and 11.76 μm × 2.6 μm, respectively. The two shift registers were fabricated on a 4000 μm × 4000 μm test chip in a 65 nm standard CMOS technology.

4.2. Test system design

The test chip is mounted on the PCB board. Apart from the board, the test system designed for irradiation experiments also includes a Zynq FPGA board and a computer, as can be seen in Fig. 10. In the Zynq FPGA chip, a PL (programmable logic) block is used to generate varying clock signal inputs for the test chip and it also receive data outputs from the test chip; a PS (processing system) block processes information between PL block and the computer via TCP/IP protocol [19].

Since the voltage for the test chip and Zynq FPGA board is 1.2 V or 3.3 V, respectively, data are not able to transmit between them directly.
Therefore, it is necessary to add a voltage champing chip and a high-speed comparator between them for level shifting, and at the same time, eliminating potential signal noise.

5. Irradiation experimental results

5.1. Laser system setup

The pulsed laser facility in the National Space Science Center (NSSC) of China was used to conduct the single event effects experiments for the proposed design and the Quatro design.

As illustrated in Fig. 11, the pulsed laser is mainly composed of the pulsed laser, the test chip, the 3D motorized stage, and the synchronization control system. By connecting the test system, the pulsed laser, and the 3D motorized stage to the synchronization control system, automatic scanning of the whole test chip can be achieved. The pulsed laser irradiates the test chip from the back side, where the test chip package was removed. Some laser parameters are listed in Table 2 [20].

5.2. Testing results

During our test, these two flip-flops chains were operated at 400 kHz with the same input pattern.

The test chip was exposed to the pulsed laser, whose energy was tuned between 60 and 360 pJ. The SEU counts and cross section data for both designs are listed in Table 3.

When the energy was either 60 or 200 pJ, only 220 flip-flops in each shift register were selected as a Region of Interests (ROI) and irradiated by the pulsed laser with the step size of 1 μm. As shown in the table, no errors were observed at the output of the proposed flip-flop chain for both laser energies. By contrast, there were 2 errors in the reference design, when the laser energy reached 200 pJ.

The laser beam with the energy of 240 pJ was used to scan these two entire shifts register chains (e.g., 4000 flip-flops) three times with the step size of 5 μm. The proposed design observed 65 errors, while the reference design saw 80 errors, i.e., 15 fewer than the former design.

Clearly, the laser data above demonstrate that the proposed design has a higher upset threshold and lower SEU cross section when compared to the reference one. As the reference Quatro design has much higher SEU tolerance than regular DFFs under heavy ion strikes [3,10], our design is also believed to have better performance under laser or heavy ion strikes.

It is interesting that the proposed design observed more errors (i.e., higher cross section) than the reference, when the laser energy was 360 pJ. More specifically, 10 more errors were observed during a single scan for the proposed design than the reference one. As the same number of black-box flip-flops (either reference or proposed design) in the shift register were irradiated with the same number of laser scans. Thus, we would expect each reference or proposed flip-flop had the same possibility of radiation strikes. As our design features larger layout and diffusion area, this results in larger cross section absolutely. This is also believed to translate to larger SEU counts for the proposed design.

6. Conclusions

The reference Quatro latch does not show complete SEU resilience in the hold state. In this paper, a novel Quatro-based latch design with low penalty is proposed. This design improves the SEU hardness through charge sharing between the additional PMOS transistors at the layout level.

It has been proven by simulations and laser experimental results that the proposed design has a larger upset threshold and lower SEU error rates, i.e., better SEU tolerance, compared with the reference structure. Further, the area and delay penalties are 13% and 37%, respectively.

Acknowledgments

This work is supported by the Fundamental Research Funds for the Central Universities (2018JB49614), NSFC through Hohai University (61504038), and Innovation Foundation of Radiation Application, China Institute of Atomic Energy (KFZC2018040205). This is also supported by Changzhou Sci & Tech Program (Grant no. CZ20180003).

References


Table 2

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Table 3

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Performance parameters of the laser device.

Table 2

Performance parameters of the laser device.

