MIL-STD-883

1 MAY 1968

MILITARY STANDARD

TEST METHODS
and
PROCEDURES
for
MICROELECTRONICS

FSC 5962

Obtained From
GLOBAL ENGINEERING DOCUMENTS
2625 So.Hickory St. Santa Ana, CA 92707
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MIL-STD-883
NOTICE 1 (USAF)
20 May 1968

MILITARY STANDARD

TEST METHODS AND PROCEDURES

FOR MICROELECTRONICS

TO ALL HOLDERS OF MIL-STD-883:

1. The following new page is to be added:

NEW PAGE	DATE
10a	20 May 1968

2. The following new methods are to be added:

NEW METHOD		DATE
T5001	Parameter Mean Value Control	20 May 1968
T5002	Parameter Distribution Control	20 May 1968
T5003	Failure Analysis Procedures For Microcircuits	20 May 1968
T5004	Screening Procedures	20 May 1968
T5005	Lot Qualification Inspection	20 May 1968
T5006	Limit Testing	20 May 1968

3. The following method pages have been revised to correct administrative errors.

REVISED PAGE	DATE	SUPERSEDED PAGE	DATE
1 (Method 1015)	20 May 1968	1 (Method 1015)	1 May 1968
2 (Method 1015)	1 May 1968	Reprinted without change	1 May 1968
1 (Method 2003)	1 May 1968	Reprinted without change	1 May 1968
2 (Method 2003)	20 May 1968	2 (Method 2003)	1 May 1968
5 (Method 2010)	1 May 1968	Reprinted without change	1 May 1968
6 (Method 2010)	20 May 1968	6 (Method 2010)	1 May 1968
7 (Method 2010).	1 May 1968	Reprinted without change	1 May 1968
8 (Method 2010)	20 May 1968	8 (Method 2010)	1 May 1968
31 (Method 2010)	20 May 1968	31 (Method 2010)	1 May 1968

4. This U. S. Air Force Notice forms a part of MIL-STD-883 dated 1 May 1968, and provides the series of test methods numbered T5001 to T5999 inclusive. Test methods in this series include primarily test sequences and procedures for applying the more specific methods of MIL-STD-883 to the general purposes of microelectronic device qualification, screening, lot acceptance and failure analysis. The general requirements, abbreviations, symbols, definitions and references of MIL-STD-883 shall apply to any application of this notice.

5. RETAIN THIS NOTICE AND INSERT BEFORE THE TABLE OF CONTENTS.

Custodians:
Air Force - 17

Review activities:
Air Force - 11, 17, 85

Preparing activity:
Air Force - 17

(Project 5962-F001)

AFLC, GAFB, N.Y., 12 Jun 68-3,000

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NUMERICAL INDEX

OF

TEST METHODS

Method No.

T5001 - Parameter mean value control
T5002 - Parameter distribution control
T5003 - Failure analysis procedures for microcircuits
T5004 - Screening procedures
T5005 - Lot qualification inspection
T5006 - Limit testing

343-218 (A-200)

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DEPARTMENT OF DEFENSE
Washington, D.C. 20360

Test methods and procedures for microelectronics

MIL-STD-883

1. This Military Standard was developed by the Department of Defense and the National Aeronautics and Space Administration.

2. This Military Standard is mandatory for use by all Departments and Agencies of the Department of Defense.

3. Recommended corrections, additions, or deletions should be addressed to Joseph Brauer, Rome Air Development Center (AFSC), Griffiss Air Force Base, New York 13440.

4. Copies of this document may be obtained from the Naval Supply Depot, 5801 Tabor Ave., Philadelphia, PA 19120.

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1. SCOPE

1.1 Purpose. This standard establishes uniform methods and procedures for testing microelectronic devices, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military and space operations, and physical and electrical tests. For the purpose of this standard, the term "devices" includes such items as monolithic, multichip, film, and hybrid microcircuits, microcircuit arrays, and the elements from which the circuits and arrays are formed. This standard is intended to apply only to microelectronic devices. The test methods described herein have been prepared to serve several purposes:

(a) To specify suitable conditions obtainable in the laboratory and at the device level which give test results equivalent to the actual service conditions existing in the field, and to obtain reproducibility of the results of tests. The tests described herein are not to be interpreted as an exact and conclusive representation of actual service operation in any one geographic or outer space location, since it is known that the only true test for operation in a specific application and location is an actual service test under the same conditions.

(b) To describe in one standard all of the test methods of a similar character which now appear in the various joint-services and NASA microelectronic device specifications, so that these methods may be kept uniform and thus result in conservation of equipment, manhours, and testing facilities. In achieving this objective, it is necessary to make each of the general tests adaptable to a broad range of devices.

(c) The test methods described herein for environmental, physical, and electrical testing of devices shall also apply, when applicable, to parts not covered by an approved Military/NASA specification, Military/NASA sheet-form standard, specification sheet, or drawing.

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2. REFERENCED DOCUMENTS

2.1 The issues of the following documents in effect on the date of invitation for bids form a part of this standard to the extent specified herein.

SPECIFICATIONS

FEDERAL

QQ-S-571 - Solder; Tin Alloy; Lead-Tin Alloy; and Lead Alloy.

MILITARY

MIL-F-14256 - Flux, Soldering, Liquid (Rosin Base).
MIL-S-19500 - Semiconductor Devices, General Specification for.
MIL-C-45662 - Calibration System Requirements.

STANDARDS

MILITARY

MIL-STD-280 - Definition of Terms for Equipment Divisions.
MIL-STD-781 - Reliability Tests, Exponential Distribution.
MIL-STD-1313 - Microelectronic Terms and Definitions.

(Copies of specifications, standards, drawings, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

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3. ABBREVIATIONS, SYMBOLS, AND DEFINITIONS

3.1 Abbreviations, symbols, and definitions. For the purpose of this standard, the abbreviations, symbols, and definitions specified in MIL-S-19500, MIL-STD-280, and MIL-STD-1313 shall apply. The following definitions shall also apply.

3.1.1 Microelectronic device. A microcircuit, microcircuit module, or an element of a microcircuit as defined in MIL-STD-1313. For the purposes of this document, each type of microelectronic device shall be identified by a unique type, part, or drawing number.

3.1.2 Mode of failure. The cause for rejection of any failed device or microcircuit as defined in terms of the specific electrical or physical requirement which it failed to meet (i.e., no failure analysis is required to identify the mode of failure, which should be obvious from the rejection criteria of the test method).

3.1.3 Mechanism of failure. The original defect which initiated the microcircuit or device failure or the physical process by which the degradation proceeded to the point of failure, identifying quality defects, internal, structural, or electrical weakness and, where applicable, the nature of externally applied stresses which led to failure.

3.1.4 Absolute maximum ratings. The values specified for ratings, maximum ratings, or absolute maximum ratings are based on the "absolute system" and are not to be exceeded under any service or test conditions. These ratings are limiting values beyond which the serviceability of any individual microelectronic integrated circuit may be impaired. It follows that a combination of all the absolute maximum ratings cannot normally be attained simultaneously. Combinations of certain ratings are permissible only if no single maximum rating is exceeded under any service or test condition. Unless otherwise specified, the voltage, current, and power ratings are based on continuous dc power conditions at free air ambient temperature of 25° ± 3°C. For pulsed or other conditions of operation of a similar nature, the current, voltage, and power dissipation ratings are a function of time and duty cycle. In order not to exceed absolute ratings, the equipment designer has the responsibility of determining an average design value, for each rating, below the absolute value of that rating by a safety factor, so that the absolute values will never be exceeded under any usual conditions of supply-voltage variations, load variations, or manufacturing variations in the equipment itself.

3.1.5 Worst case condition. Worst case condition(s) consists of the simultaneous application of the most adverse (in terms of required function of the device) values (within the stated operating ranges) of bias(es), signal input(s), loading and environment to the device under test. Worst cases for different parameters may be different. If all the applied test conditions are not established at the most adverse values, the term "partial worst case condition" shall be used to differentiate and shall be accompanied by identification of the departure from worst case. For example, the lowest values of supply voltages, signal input levels, and ambient temperature and the highest value of loading may constitute "worst case conditions" for measurement of the output voltage of a gate. Use of the most adverse values of applied electrical conditions, at room temperature, would then constitute "partial worst case conditions" and shall be so identified using a postscript "at room temperature."

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4. GENERAL REQUIREMENTS

4.1 Numbering system. The test methods are designated by numbers assigned in accordance with the following system:

4.1.1 Classification of tests. The tests are divided into four classes: test methods numbered 1001 to 1999 inclusive, cover environmental tests; those numbered 2001 to 2999 inclusive, cover mechanical tests; those numbered 3001 to 4999 inclusive, cover electrical tests. Within each class, test methods and procedures are serially numbered in the order in which they are introduced into this standard.

4.1.2 Revisions. Revisions are numbered consecutively using a period to separate the test method number and the revision number. For example, 4001.1 is the first revision of test method 4001.

4.2 Method of reference. When applicable, test methods contained herein shall be referenced in the individual specification by specifying this standard, the method number, and the details required in the summary paragraph of the applicable method. To avoid the necessity for changing specifications which refer to this standard, the revision number should not be used when referencing test methods. For example, use 4001, not 4001.1.

4.3 Test conditions. Unless otherwise specified herein, or in the applicable procurement documentation, all measurements and tests shall be made at ambient temperature of 25° ± 3°C and at ambient atmospheric pressure and relative humidity. Whenever these conditions must be closely controlled in order to obtain reproducible results, the referee conditions shall be as follows: temperature 25° ± 1°C, relative humidity 50 ± 5 percent, and atmospheric pressure from 650 to 800 millimeters of mercury.

4.3.1 Permissible temperature variation in environmental chambers. When chambers are used, specimens under test shall be located only within the working area defined as follows:

(a) Temperature variation within working area: The controls for the chamber shall be capable of maintaining the temperature of any single reference point within the working area within ±2°C or 4 percent, whichever is greater.

(b) Space variation within working area: Chambers shall be so constructed that at any given time, the temperature of any point within the working area shall not deviate more than ±3°C or ±3 percent, whichever is greater, from the reference point, except for the immediate vicinity of specimens generating heat.

4.3.2 Electrical test frequency. Unless otherwise specified, the electrical test frequency shall be the specified operating frequency. Where a frequency range is specified, major functional parameters shall be tested at the maximum and minimum frequencies of the range in addition to those tests conducted at any specified frequency within the range. Whenever electrical tests are conducted on microelectronic devices for which a range of frequencies or more than a single operating frequency is specified, the frequency at which tests are conducted shall be recorded along with the parameters measured at those frequencies.

4.3.3 Accuracy. The specified limits are for absolute (true) values obtained with the specified (nominal) test conditions. Proper allowance shall be made for measurement errors (including those due to deviations from nominal test conditions) in establishing the working limits to be used for the measured values so that the true values of the device parameters (as they would be under nominal test conditions) are within the specified limits.

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4.3.4 Calibration. Calibration of all test equipment used in the production control and testing (including electrical test equipment, environmental equipment controls and other instrumentation) shall be in accordance with MIL-C-45662 and the following requirements. All electrical test equipment shall be calibrated at periodic intervals and all acceptable equipment shall display a record of the calibration dates and responsible individual or activity. The interval shall be based upon the class of equipment and its history. All automatic test equipment or other electrical test equipment employed in qualification, acceptance, life demonstration, and similar repetitive testing shall receive a calibration check at least every calendar week employing controlled sample microelectronic devices of the type being tested or test standards traceable to the National Bureau of Standards. Calibration check readings shall agree with the values recorded for each control device within the accuracy requirements of 4.3.3.

4.3.5 Data reporting. The data resulting from application of any test method or procedure shall be reported in terms of the actual test conditions and results. "Equivalent" results (e.g., equivalent 25°C device hours or failure rates derived from 125°C test conditions) may be reported in addition to the actual results but shall not be acceptable as an alternative to actual results. Results of any test method or procedure shall be accompanied by information on the total quantity of devices in each lot being tested on a 100 percent or sampling basis, the associated quantity of devices in the sample for tests on a sampling basis, and the number of failures or devices rejected by test method and observed mode of failure. In cases where more than a single device type (part number) is involved in the makeup of a lot for inspection or delivery, the data shall be reported as above but with a further breakdown by part number.

4.3.6 Test sample disposition. Unless otherwise specified in the applicable procurement document, and except for those test methods and procedures specifically employed as 100 percent screens or 100 percent acceptance tests, devices which survive the test methods described in this standard, shall not be acceptable for shipment.

4.4 Orientation. For those test methods which involve observation or the application of external forces which must be related to the orientation of the device, such orientation and direction of forces applied shall be identified in accordance with figures 1 and 2 below:

NOTE: For case configurations other than those shown in figures 1 and 2, the orientation of the device shall be as specified in the applicable procurement document.

NOTE: In flat packages where radial leads emanate from 3 or more sides, the X-direction shall be assigned to the larger and the Z-direction to the smaller of the two lateral dimensions.

4.5 General precautions. The following precautions shall be observed in the testing of devices:

4.5.1 Transients. Devices shall not be subjected to conditions in which voltage or current transients cause the ratings to be exceeded.

4.5.2 Test conditions for electrical measurements. Test conditions for all nondestructive electrical measurements should be such that maximum ratings are not exceeded. The precautions should include limits on maximum instantaneous currents and applied voltages.

4.5.3 Test methods and circuits. Unless otherwise stated in the specific test method, the methods and circuits shown are given as the basic measurement method. They are not necessarily the only method or circuit which can be used, but the manufacturer shall demonstrate to the procuring activity that alternate methods or circuits which he may desire to use are equivalent and give results within the desired accuracy of measurement (see 4.3.3).

4.5.4 Soldering and welding. Adequate precautions shall be taken to avoid damage to the device during soldering or welding required for tests.

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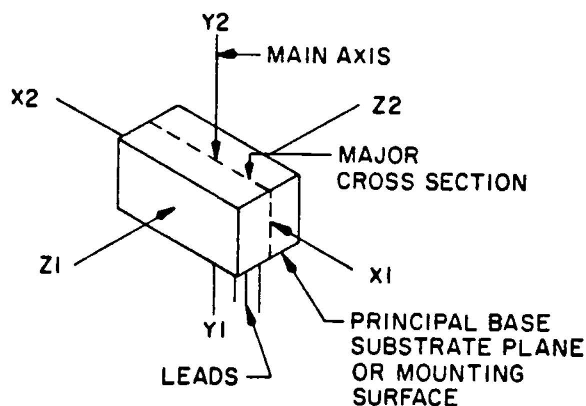

FIGURE 1a. Orientation of microelectronic device to direction of applied force.

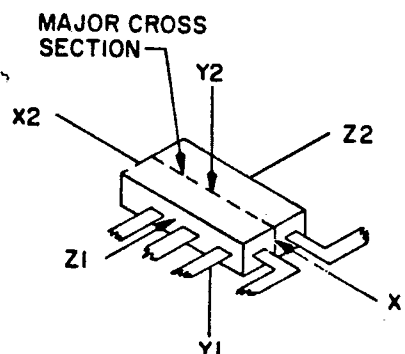

FIGURE 1b. Radial lead flat packages.

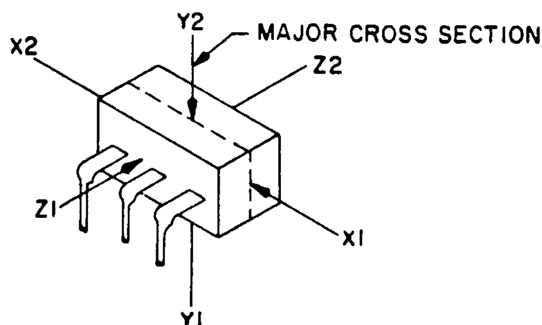

FIGURE 1c. Dual in-line package.

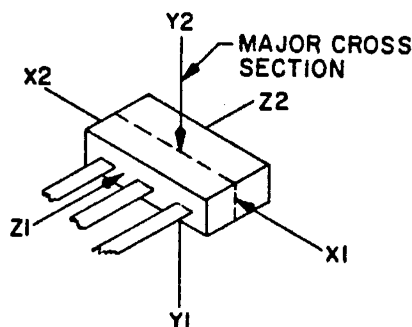

FIGURE 1d. Flat package with radial leads from one side only.

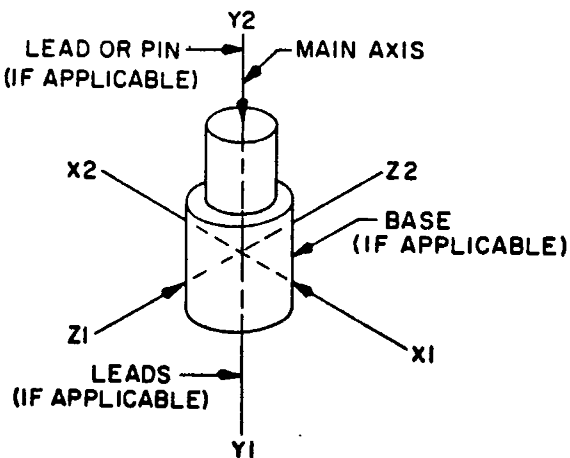

FIGURE 2. Orientation of cylindrical microelectronic device to direction of applied force.

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4.5.5 Order of connection of leads. Care should be taken when connecting a microelectronic device to a power source. For MOS devices or other microelectronic circuits or devices where the order of connection of leads may be important, precautions cited in the applicable procurement document shall be observed.

4.5.6 Radiation precautions. Due precautions shall be used in storing or testing microelectronic devices in substantial fields of x-rays, neutrons, or other energy particles.

4.5.7 Handling precautions for microelectronic devices.

(a) Ground all equipment prior to insertion of the device for electrical test.
(b) Where applicable, keep devices in metal shields until they are inserted in the equipment or until necessary to remove for test.
(c) Where applicable, keep devices in carriers or other protective packages during test.

4.5.8 Control of junction temperature. Where the application of the specified electrical inputs during test will cause the device or any internal junction temperature (T_J) to differ from the specified test temperature, case temperature (T_C), or ambient temperature (T_A) by more than ±2°C, the following precautions shall be observed, as applicable: Where it is required that $T_J = T_A$ or T_C, the device shall be temperature stabilized in the power-off condition until the device temperature is within ±2°C of the case or ambient temperature, as applicable, and the prescribed power-on measurement shall be made as quickly as possible (and in no case in excess of 30 seconds) after the application of electrical inputs. Where it is required that T_J reach a normal operating level in excess of T_A or T_C, the device shall be stabilized for a sufficient period of time in a power-on condition with all specified electrical inputs applied to allow T_J to reach a temperature of at least 80 percent of its stable value under the specified test conditions.

4.5.9 Testing of multiple input/output devices. Where any input or output parameter is specified for devices having more than a single input or output, the specified parameter shall be tested at all input or output terminations of the device.

4.5.10 Testing of complex devices. Where microelectronic devices being tested contain multiple circuits or functions, whether independently connected to the external device leads or whether internally connected in some arrangement to minimize the number of external leads, suitable test circuits and procedures shall be applied so as to test all circuits or functions contained in the device with all the applicable test methods specified in the applicable procurement document. For example, if a device contains a pair of logic gates it shall not be acceptable to test only one of the gates for the specified parameters. Furthermore, multiple circuit devices should be tested to assure that no significant interaction exists between individual circuits (e.g., application of signal to one gate of a dual gate device should not cause a change in output of the other gate). The intent of this requirement is to assure that all circuit elements in a microelectronic device are exercised to the fullest extent allowed by their construction and connection provisions. For circuit arrays containing complex signal paths which vary depending on the nature of incoming signals or internal functions performed on the incoming signals, this requirement shall be met by programming the operation of the device to assure that all circuit elements are caused to function and thus provide the opportunity to observe or measure the levels of their performance in accordance with the specified test methods.

Custodians:
Air Force - 17
Army - EL
Navy - EC
NASA - HQ (KR)

Reviewer:
Air Force - 11, 17, 85
Army - EL, MI, MU
Navy - EC, SH
NASA - HQ (KR)
DSA - ES

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Users:
Air Force - 19
Army - EL, SM
Navy - CG, MC, AS, OS
NASA - HQ (KR)

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NUMERICAL INDEX

OF

TEST METHODS

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Method No.	Title
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APPENDIX

TEST METHODS

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METHOD 1001

BAROMETRIC PRESSURE, REDUCED (ALTITUDE OPERATION)

1. PURPOSE. The barometric-pressure test is performed under conditions simulating the low atmospheric pressure encountered in the nonpressurized portions of aircraft and other vehicles in high-altitude flight. This test is intended primarily to determine the ability of component parts and materials to avoid voltage breakdown failures due to the reduced dielectric strength of air and other insulating materials at reduced pressures. Even when low pressures do not produce complete electrical breakdown, corona and its undesirable effects, including losses and ionization, are intensified. The simulated high-altitude conditions of this test can also be employed to investigate the influence on components' operating characteristics, of other effects of reduced pressure, including changes in dielectric constants of materials, and decreased ability of thinner air to transfer heat away from heat-producing components.

2. APPARATUS. The apparatus used for the barometric-pressure test shall consist of a vacuum pump and a suitable sealed chamber having means for visual observation of the specimen under test when necessary, a suitable pressure indicator to measure the simulated altitude in feet in the sealed chamber, and a microammeter or oscilloscope capable of detecting current over the range from DC to 30 megahertz.

3. PROCEDURE. The specimens shall be mounted in the test chamber as specified and the pressure reduced to the value indicated in one of the following test conditions, as specified. While the specimens are maintained at the specified pressure, the specimens shall be subjected to the specified tests. During this test and for a period of 20 minutes before, the test temperature shall be 25° ±10° C. The device shall have the specified voltage applied and shall be monitored over the range from atmospheric pressure to the specified minimum pressure and return for any device malfunctions. A device which exhibits arc-overs, harmful coronas, or any other defect or deterioration which may interfere with the operation of the device shall be considered a failure.

Test condition	Pressure, maximum		Altitude	
	Inches of mercury	mm of mercury	Feet	Meters
A - - - - - - - - - -	17.3	439.00	15,000	4,572
B - - - - - - - - - -	8.88	226.00	30,000	9,144
C - - - - - - - - - -	3.44	87.00	50,000	15,240
D - - - - - - - - - -	1.31	33.00	70,000	21,336
E - - - - - - - - - -	0.315	8.00	100,000	30,480
F - - - - - - - - - -	0.043	1.09	150,000	45,720
G - - - - - - - - - -	9.436×10^{-8}	2.40×10^{-6}	656,000	200,000

3.1 Measurement. The device shall be connected for measurement and have the specified voltages applied during the entire pump-down cycle. The terminals to which the maximum voltage (see 4(c)) is applied shall be monitored with a microammeter or oscilloscope for corona currents in the range from DC to 30 megahertz. Provision shall be made for calibrating the current flow in the test circuit minus the device under the applicable test condition to insure that test readings are characteristic of the device under test.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Method of mounting (see 3).
(b) Test condition letter (see 3). Unless otherwise specified, Condition E shall be used.
(c) Tests during subjection to reduced pressure (see 3). Unless otherwise specified, the device shall be subjected to the maximum voltage it would be subjected to under rated operating conditions.

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METHOD 1001 - Continued

(d) Tests after subjection to reduced pressure, if applicable (see 3). Unless otherwise specified, the device shall be subjected to full electrical tests of specified device characteristics or parameters.
(e) Exposure time prior to measurement, if applicable (see 3).

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METHOD 1002

IMMERSION

1. PURPOSE. This test is performed to determine the effectiveness of the seal of microelectronic devices. The immersion of the part under evaluation into liquid at widely different temperatures subjects it to thermal and mechanical stresses which will readily detect a defective terminal assembly, or a partially closed seam or molded enclosure. Defects of these types can result from faulty construction or from mechanical damage such as might be produced during physical or environmental tests. The immersion test is generally performed immediately following such tests because it will tend to aggravate any incipient defects in seals, seams, and bushings which might otherwise escape notice. This test is essentially a laboratory test condition, and the procedure is intended only as a measurement of the effectiveness of the seal following this test. The choice of fresh or salt water as a test liquid is dependent on the nature of the component part under test. When electrical measurements are made after immersion cycling to obtain evidence of leakage through seals, the use of a salt solution instead of fresh water will facilitate detection of moisture penetration. This test provides a simple and ready means of detection of the migration of liquids. Effects noted can include lowered insulation resistance, corrosion of internal parts, and appearance of salt crystals. The test described is not intended as a thermal-shock or corrosion test, although it may incidentally reveal inadequacies in these respects. This is a destructive test and shall not be used as a 100 percent test or screen.

2. APPARATUS. The apparatus used for the immersion test shall consist of controlled temperature baths capable of maintaining the temperatures indicated for the hot bath and the cold bath test condition selected. A suitable temperature indicator shall be used to measure bath temperature.

3. PROCEDURE. This test consists of successive cycles of immersions, each cycle consisting of immersion in a hot bath of fresh (tap) water at a temperature of $65^\circ {}^{+5^\circ}_{-0^\circ}$ C followed by immersion in a cold bath. The number of cycles, duration of each immersion, and the nature and temperature of the cold bath shall be as indicated in the applicable test condition listed below, as specified. The transfer of specimens from one bath to another shall be accomplished as rapidly as practicable and in no case shall transfer time exceed 15 seconds. After completion of the final cycle, specimens shall be thoroughly and quickly washed in fresh (tap) water or distilled water and all surfaces wiped or air-blasted clean and dry. Unless otherwise specified, measurements shall be made at least 4 hours, but not more than 48 hours, after completion of the final cycle. When specified in the applicable procurement document, upon completion of the electrical measurements and external visual examination, the device shall be delidded or dissected and examined in accordance with method 2013 for evidence of corrosion of internal elements or the appearance of salt crystals. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

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METHOD 1002 - Continued

Test condition	Number of cycles	Duration of each immersion Minutes	Immersion bath (cold)	Temperature of cold bath °C
A - - - - - - - - -	2	15	Fresh (tap) water	25^{+10}_{-5}
B - - - - - - - - -	2	15	Saturated solution of sodium chloride and water	25^{+10}_{-5}
C - - - - - - - - -	5	60	Saturated solution of sodium chloride and water	0 ± 3
D - - - - - - - - -	5	60	(Parts by Volume) Water - 48 parts Methanol*- 50 parts Morpholine - 1 part 3.5-dimethyl-1-hexyn-3-ol-1 part Stannous chloride - 5 grams	0 ± 3

* Synonyms are tetrahydro-1, 4-oxazine and diethylenimide oxide.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Test-condition letter (see 3). Unless otherwise specified, condition C shall be used.
(b) Time after final cycle allowed for measurements, if other than that specified (see 3).
(c) Measurements after final cycle (see 3). Unless otherwise specified, measurements shall include pin-to-pin resistance, pin-to-case resistance and full electrical test of all device characteristics or parameters listed in the applicable procurement document. Final evaluation shall include external visual examination for legibility of device markings and for evidence of discoloration or corrosion of package and leads.
(d) Dissection and internal examination, where applicable (see 3).

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METHOD 1003

INSULATION RESISTANCE

1. PURPOSE. This test is to measure the resistance offered by the insulating members of a component part to an impressed direct voltage tending to produce a leakage of current through or on the surface of these members. Insulation-resistance measurements should not be considered the equivalent of dielectric withstanding voltage or electric breakdown tests. A clean, dry insulation may have a high insulation resistance, and yet possess a mechanical fault that would cause failure in the dielectric withstanding voltage test. Since insulating members composed of different materials or combinations of materials may have inherently different insulation resistances, the numerical value of measured insulation resistance cannot properly be taken as a direct measure of the degree of cleanliness or absence of deterioration.

1.1 Factors affecting use. Factors affecting insulation-resistance measurements include temperature, humidity, residual charges, charging currents or time constant of instrument and measured circuit, test voltage, previous conditioning, and duration of uninterrupted test voltage application (electrification time). In connection with this last-named factor, it is characteristic of certain components (for example, capacitors and cables) for the current to usually fall from an instantaneous high value to a steady lower value at a rate of decay which depends on such factors as test voltage, temperature, insulating materials, capacitance, and external circuit resistance. Consequently, the measured insulation resistance will increase for an appreciable time as test voltage is applied uninterruptedly. Because of this phenomenon, it may take many minutes to approach maximum insulation-resistance readings, but specifications usually require that readings be made after a specified time. This shortens the testing time considerably while still permitting significant test results, provided the insulation resistance is reasonably close to steady-state value, the current versus time curve is known, or suitable correction factors are applied to these measurements. For certain components, a steady instrument reading may be obtained in a matter of seconds. When insulation-resistance measurements are made before and after a test, both measurements should be made under the same conditions.

2. APPARATUS. Insulation-resistance measurements shall be made on an apparatus suitable for the characteristics of the component to be measured such as a megohm bridge, megohmmeter, insulation-resistance test set, or other suitable apparatus.

3. PROCEDURE. When special preparations or conditions such as special test fixtures, reconnections, grounding, isolation, low atmospheric pressure, humidity, or immersion in water are required, they shall be specified. Insulation-resistance measurements shall be made between the mutually insulated points or between insulated points and ground, as specified. When electrification time is a factor, the insulation-resistance measurements shall be made immediately after the specified time (see 4) of uninterrupted test voltage application, unless otherwise specified. However, if the instrument-reading indicates that an insulation resistance meets the specified limit, and is steady or increasing, the test may be terminated before the end of the specified period. When more than one measurement is specified, subsequent measurements of insulation resistance shall be made using the same polarity as the initial measurements. Unless otherwise specified, the direct potential applied to the specimen shall be that indicated by one of the test-condition letters, as specified below, and insulation resistance measurements shall be made with both polarities of the applied voltage:

Test condition	Test potential
A	10 volts ± 10%
B	25 volts ± 10%
C	50 volts ± 10%
D	100 volts ± 10%
E	500 volts ± 10%
F	1,000 volts ± 10%

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METHOD 1003 - Continued

For inplant quality conformance testing, any voltage may be used provided it is equal to or greater than the minimum potential allowed by the applicable test condition. Unless otherwise specified, the measurement error at the insulation-resistance value shall not exceed 10 percent. Proper guarding techniques shall be used to prevent erroneous readings due to leakage along undesired paths.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Test-condition letter, or other test potential, if specified (see 3).
(b) Special preparations or conditions, if required (see 3).
(c) Points of measurement (see 3). Unless otherwise specified, insulation resistance shall be measured between the device leads (all leads electrically connected to each other or to a common point) and the device case, and the measured resistance shall be no less than 15 megohms.
(d) Electrification time, if critical (see 1.1).
(e) Insulation resistance in terms of maximum leakage current at a specified test voltage. Unless otherwise specified, the maximum leakage between any adjacent disconnected leads shall not exceed 100 nanoampere at 100 volts DC.

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METHOD 1004

MOISTURE RESISTANCE

1. PURPOSE. The moisture-resistance test is performed for the purpose of evaluating, in an accelerated manner, the resistance of component parts and constituent materials to the deteriorative effects of the high-humidity and heat conditions typical of tropical environments. Most tropical degradation results directly or indirectly from absorption of moisture vapor and films by vulnerable insulating materials, and from surface wetting of metals and insulation. These phenomena produce many types of deterioration, including corrosion of metals; physical distortion and decomposition of organic materials; leaching out and spending of constituents of materials; and detrimental changes in electrical properties. This test differs from the steady-state humidity test and derives its added effectiveness in its employment of temperature cycling, which provides alternate periods of condensation and drying essential to the development of the corrosion processes and, in addition, produces a "breathing" action of moisture into partially sealed containers. Increased effectiveness is also obtained by use of a higher temperature, which intensifies the effects of humidity. The test includes low-temperature and vibration subcycles that act as accelerants to reveal otherwise undiscernible evidences of deterioration since stresses caused by freezing moisture and accentuated by vibration tend to widen cracks and fissures. As a result the deterioration can be detected by the measurement of electrical characteristics (including such tests as voltage breakdown and insulation resistance) or by performing of a test for sealing. Provision is made for the application of a polarizing voltage across insulation to investigate the possibility of electrolysis, which can promote eventual dielectric breakdown. This test also provides for electrical loading of certain components, if desired, in order to determine the resistance of current-carrying components, especially fine wires and contacts, to electro-chemical corrosion. Results obtained with this test are reproducible and have been confirmed by investigations of field failures. This test has proved reliable for indicating those parts which are unsuited for tropical field use.

2. APPARATUS. The apparatus used for the moisture resistance test shall include temperature-humidity chambers and vibration equipment capable of maintaining the cycles and tolerances described in figures 1004-1 or 1004-2 and electrical test equipment capable of performing the measurements in paragraph 3.6 and paragraph 4.

3. PROCEDURE. Specimens shall be tested in accordance with 3.1 thru 3.6 inclusive, and figures 1004-1 or 1004-2. Specimens shall be mounted in a manner that will expose them to the test environment. When this test is performed as part of a group or subgroup of tests where lead integrity tests in accordance with method 2004, test conditions B1 and C1 are conducted prior to exposure to this test, the initial conditioning (see 3.1) may be omitted. When a group or subgroup of tests is performed which includes testing in accordance with more than a single test method where the initial conditioning requirements (see 3.1) are imposed, the conditioning shall be applied only once prior to the performance of these methods and shall be omitted from the succeeding test method(s).

3.1 Initial conditioning. Prior to mounting specimens for the moisture resistance test, the device leads shall be subjected to bending and torsion stresses. Each lead of each specimen shall be exposed to the following stresses:

(a) Lead bend. A force of 8.0 ± 1.0 oz, unless otherwise specified, shall be applied to the lead at a distance of 0.12 ± 0.03 inch from the device body or at the end of the lead if it is shorter than 0.12 in. The force shall be applied to each lead once in each of two mutually perpendicular directions, both directions being perpendicular to the original lead position. When devices have leads which are formed close to the body, the forces may be applied 0.12 ± 0.03 inch from the form. Bending force shall be applied in accordance with the applicable diagram of figure 2004-1, method 2004 of this standard. For a device lead which bends noticeably when less than the specified force is applied, the bend shall be continued until the specified force is achieved or until the bend equals 90^{+10}_{-0} degrees, whichever condition

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METHOD 1004 - Continued

occurs first. The lead shall then be restored to its original position. For ribbon lead flat packs (such as the TO-84 and TO-89 packages) where the lead cross section is 0.002 x 0.020 inches or less and the width to thickness ratio is greater than 8 to 1, a force of 3 ± 0.3 ounces shall be applied instead of the 8 ounce force specified above and the lead bend conditioning shall not be applied to the end leads of packages (such as the TO-89 package) where the application of the bending stress will apply primarily torsion at the lead seal.

(b) Lead torsion. A torque of 2.0 ± 0.2 oz-in., unless otherwise specified, shall be applied to the lead at a distance of 0.12 ± 0.03 inch from the device body or at the end of the lead if it is shorter than 0.12 inch. The torque shall be applied about the axis of the lead once in each direction (clockwise and counterclockwise). When devices have leads which are formed close to the body, the torque may be applied 0.12 ± 0.03 inch from the form. Torque shall be applied in accordance with the applicable diagram of figure 2004-2, test method 2004 of this standard. For device leads which twist noticeably when less than the specified torque is applied, the twist shall be continued until the specified torque is achieved or until the twist equals $30° {}^{+10}_{-0}$ degrees, whichever condition occurs first. The lead shall then be restored to its original position.

3.2 Initial measurements. Prior to step 1 of the first cycle, the specified initial measurements shall be made at room ambient conditions, or as specified.

3.3 Number of cycles. Specimens shall be subjected to 10 continuous cycles, each as shown on figure 1004-1 or 1004-2.

3.4 Subcycle. During step 7, at least 1 hour but not more than 4 hours after step 7 begins, the specimens shall be either removed from the humidity chamber, or the temperature of the chamber shall be reduced, for performance of step 7a. After step 7b, the specimens shall be returned to 25°C at 90 to 98 percent relative humidity (RH) and kept there until the next cycle begins. This subcycle shall be performed during any five of the first nine cycles.

3.4.1 Step 7a. At least 1 hour but not more than 4 hours after the beginning of step 7, the specimens shall be either removed from the humidity chamber, or the temperature of the chamber shall be reduced. Specimens shall then be conditioned at -09° ±2°C, with humidity not controlled, for 3 hours as indicated on figure 1004-1 or 1004-2. When a separate cold chamber is not used, care should be taken to assure that the specimens are held at -10° ±2°C, for the full 3-hour period.

3.4.2 Step 7b. Within 15 minutes after completion of step 7a and with humidity not controlled, specimens shall be vibrated for 15 minutes, at room ambient temperature, using a simple harmonic motion having an acceleration between 20 and 50g, the frequency being varied uniformly between the approximate limits to 50 and 2,000 hertz (Hz). The entire frequency range, from 50 to 2,000 Hz and return to 50 Hz, shall be traversed in approximately one minute.

3.5 Applied voltage. During the moisture resistance test as specified in figure 1004-1 or 1004-2, when applicable (see 4), the device shall have a voltage difference equal to the nominal rated bias voltage applied between any two adjacent leads or, as an alternative, shall have all leads biased for normal operation.

3.6 Final measurements.

3.6.1 At high humidity. Upon completion of step 6 of the final cycle, when measurements at high humidity are specified, the specimens shall be maintained at a temperature of 25° ±2°C and an RH of 90 to 98 percent for a period of 1-1/2 to 3-1/2 hours, and the specified measurements shall be made within 2 hours after removal from the chamber. Due to the difficulty in making measurements

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under high-humidity conditions, the individual specification shall specify the particular precautions to be followed in making measurements under such conditions.

3.6.2 After drying period. Following step 6 of the final cycle, or following measurements at high humidity if applicable, specimens may be conditioned for up to 24 hours at the ambient conditions specified for the initial measurements (see 3.2) after which the specified measurements shall be made. Failures shall be recorded as of the time of first measurement, and, where applicable, at any subsequent measurement times up to a maximum of 24 hours.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Initial measurements, and conditions if other than room ambient (see 3.2).
(b) Applied voltage when applicable (see 3.5).
(c) Measurements at high humidity, when applicable (see 3.6.1) and precautions as applicable.
(d) Final measurements (see 3.6). Unless otherwise specified, final measurements shall include all specified electrical characteristics and parameters.

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METHOD 1004 - Continued

FIGURE 1004-1. Graphical representation of moisture-resistance test.

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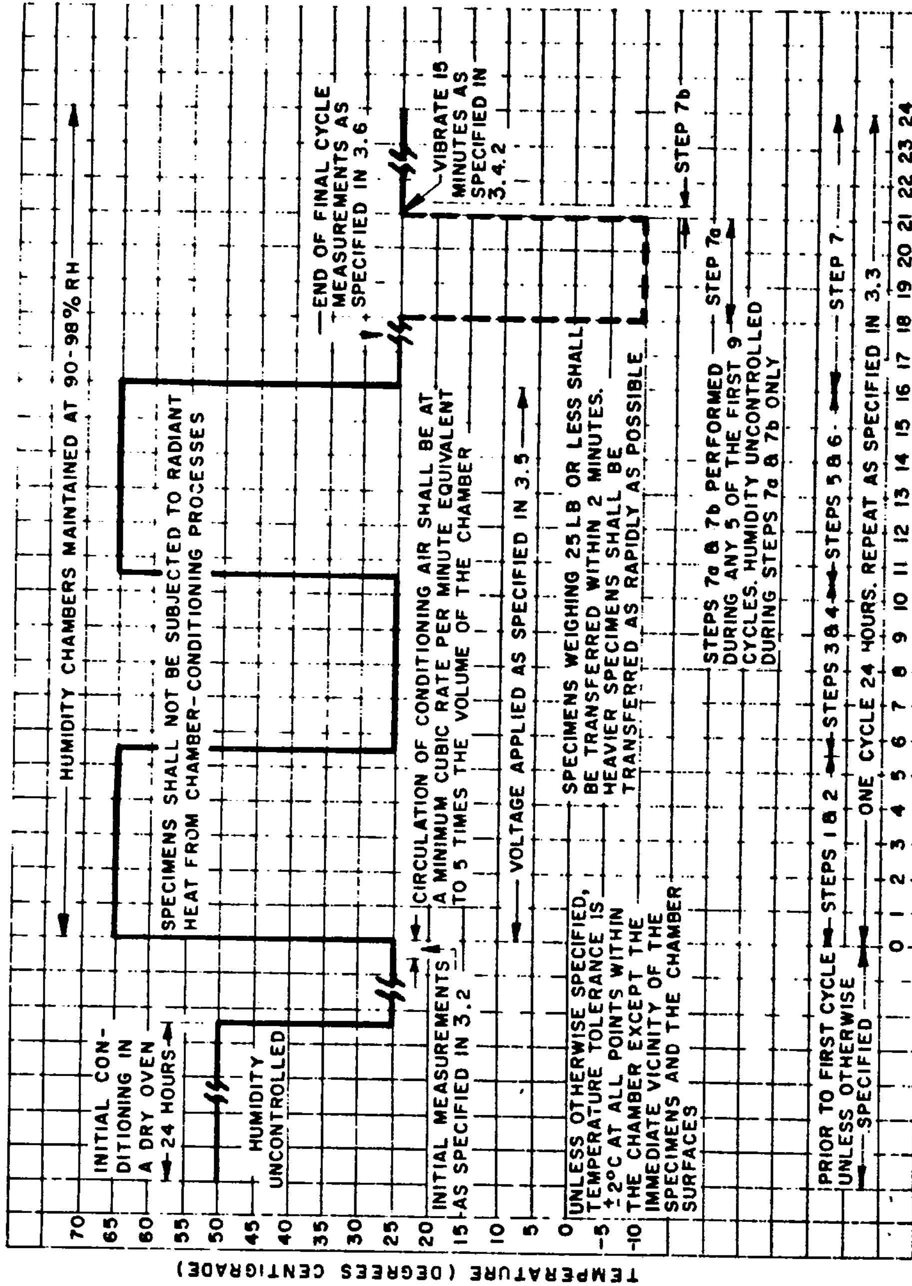

FIGURE 1004-2. Graphical representation of moisture-resistance test (alternate method).

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METHOD 1005

STEADY STATE LIFE

1. PURPOSE. The steady state life test is performed for the purpose of determining a representative failure rate (λ) for microelectronic devices or demonstrating the quality or reliability of devices subjected to the specified conditions. Failure rates are ordinarily determined either for general qualification of devices, for the production lines from which they are obtained or for the purpose of predicting the failure rates (or MTBF) of equipments in which the devices are to be employed. In the case of general qualification testing, it must be assumed that the devices may be applied under any combination of stress or environment up to their maximum operating ratings. Where the test is directed at the capability of the device in a particular equipment application, the test conditions of primary interest may be at levels lower than the maximum device ratings. For use in equipment failure-rate predictions, it is frequently desirable to establish device failure rates for other than the maximum rated conditions. While there is considerable variation between failure rates observed in tests of relatively short duration on microelectronic devices of varying pretest histories, the results of longer term tests generally assume more reproducible values and indicate a trend of decreasing failure rate with time. A failure rate decrease which is more rapid at the higher stress levels implies a trend due to the continual screening-out of defective devices (incipient failures) or those with characteristically less resistance to degradation or catastrophic failure than the typical device. Life tests should be conducted for a sufficiently long test period to assure that results are not characteristic of early failures or "infant mortality" and periodic observations of results should be made prior to the end of the life test to provide an indication of any significant variation in failure rate with time. Valid results at these shorter intervals require a sufficiently large sample size to provide a reasonable probability of detection of failures in the sample corresponding to the distribution of potential failures in the lot(s) from which the sample was drawn. The test conditions provided in 3 below are intended to reflect these considerations.

When this test is employed for the purpose of assessing the general capability of a device or for device qualification tests in support of unspecified future applications, the test conditions shall be selected so as to represent the maximum operating ratings of the device in terms of electrical input(s), output(s), load and bias and the corresponding maximum operating temperature or other specified environment. When this test is employed to evaluate the capability of the device over a range of stresses or environments, test conditions shall be selected so as to represent the maximum and minimum stresses or environments for the range of interest. Where it is expected or observed in initial tests that measured failure rates for these extreme conditions differ by more than one order of magnitude, tests shall be conducted at intermediate levels so as to acquire data points which are in no case separated by more than one order of magnitude in failure rates. It is considered reasonable to interpolate continuous plots of failure rate versus stress level where the range of interpolation is bounded on both ends by data points which differ by less than one order of magnitude.

2. APPARATUS. The apparatus required for the accomplishment of this test shall consist of suitable chambers to maintain the devices at specified test temperature and provide access to specified electrical connections, and appropriate electrical test equipment to provide the required electrical inputs and perform the specified intermediate and endpoint measurements.

3. PROCEDURE. The microelectronic device shall be subjected to the steady state life test at the temperature and for the time specified. The device shall be operated under the specified test condition (see 3.4). Lead, stud or case mounted devices shall be mounted by the leads, stud or case in their normal mounting configuration and the point of connection shall be maintained at a temperature not less than the specified temperature. The test condition, duration, sample size and temperature selected prior to test shall be recorded and shall govern for the entire test.

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METHOD 1005 - Continued

3.1 Test duration. Unless otherwise specified, the life test duration shall be no less than 1,000 hours for any microelectronic device or test condition. Where devices have been subjected prior to this test, to special screening, burn-in, elevated temperature storage or any preconditioning treatment which is not done as a routine production line procedure on the type and grade of device being tested, it may be desirable to increase the minimum test duration to 2,000 hours (see 4(c)). In order to achieve a truly representative failure rate, it is obviously desirable to continue the test for sufficient time to achieve at least one and preferably three or four failures. Where the purpose of this test is to demonstrate compliance with a specified lambda (λ), the test may be terminated at the point of rejection if this occurs prior to the minimum test durations specified above.

3.2 Measurements. End point measurements shall be made at 0 hours and at the specified end point $^{+72}_{-24}$ hours and shall consist of all specified end point electrical parameters (including parameters specified at temperature extremes). Intermediate measurements shall be made at 168 $^{+72}_{-0}$ hours, and 504 $^{+72}_{-0}$ hours for tests of 1,000 hours duration. For tests of 2,000 hours duration, intermediate measurements shall be made at 168 $^{+72}_{-0}$ hours, 504 $^{+72}_{-0}$ hours, 1,000 $^{+72}_{-24}$ hours, and 1,500 $^{+72}_{-24}$ hours. For tests continued in excess of 2,000 hours duration, measurements shall be made at the intermediate points specified for the 2,000 hour test and at each succeeding 1,000 $^{+72}_{-24}$ hours interval. These intermediate measurements shall consist of the major functional characteristics of the device under test sufficient to reveal both catastrophic and degradation failures to specified limits, and may be conducted either while the devices are at test temperature or at 25 $^{+3}_{-0}$ °C upon removal of the devices from the test chamber. When devices are measured at 25°C following application of test conditions A or C, they shall be cooled from the test temperature to 25°C prior to removal of bias voltage(s) and all specified electrical measurements shall be completed within 8 hours from the time bias is removed.

3.3 Test sample. The test sample shall be as specified (see 4). When this test method is employed as an add-on life test for a series or family of device types, lesser quantities of any single device type may be introduced in any single addition to the total sample quantity, but the results shall not be considered valid until the minimum sample size for each device type has been accumulated. Where all or part of the samples previously under test are extracted upon addition of new samples, the minimum sample size for each type shall be maintained once that level is initially reached and no sample shall be extracted until it has accumulated the specified minimum test hours (see 3.1).

3.4 Test conditions. The microelectronic devices shall be subjected to the specified test condition as described below and in the applicable procurement document for the specified time and temperature and the required measurements shall be made at the specified intermediate points and end points.

(a) Test condition A. Steady-state, reverse bias. This test condition is illustrated in figure 1005-1 and is suitable for use on all types of circuits, linear or digital types. In this test as many junctions as possible shall be reverse biased to the specified voltage and power dissipation. The ambient test temperature shall be the maximum possible but shall be selected so as not to exceed the thermal rating of the device.

(b) Test condition B. Steady-state, power. This test condition is illustrated in figure 1005-1 and can be used on all digital type circuits and on some linear types. In this test, as many junctions as possible shall be forward biased as specified. The ambient test temperature shall be the maximum possible but shall be selected so as not to exceed the thermal rating of the device.

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METHOD 1005 - Continued

(c) Test condition C. Steady-state, power and reverse bias. This test condition is illustrated in figure 1005-1 and is used strictly on digital type circuits where the inputs can be reverse biased and the output can be biased for maximum power dissipation or vice versa. The ambient temperature shall be selected so as not to exceed the maximum thermal rating of the device.

(d) Test condition D. Parallel excitation. This test condition is illustrated in figure 1005-2 and is suitable for use on all circuit types. Each circuit is driven with an appropriate signal to simulate as closely as possible circuit application. All circuits shall have a maximum load applied, excitation shall be applied at a frequency of no less than 60 Hz, and the test shall be conducted at the maximum rated temperature, unless otherwise specified. This test is usually referred to as parallel switching applied to digital circuits.

(e) Test condition E. Ring oscillator. In this test, illustrated in figure 1005-3, any number of digital circuits greater than two are connected in series. For circuits that cause phase inversion, an odd number of circuits should be used with the output of the last circuit connected to the input of the first circuit. The series will be free running at a frequency established by the propagation delay of each circuit and its associated wiring. Each circuit in the ring shall be loaded to its rated maximum and biased at normal rated voltage. The test shall be conducted at maximum rated temperature unless otherwise specified. This test may be conducted with the open-ring or series switching configuration where the first device in the series is switched by an external source. In this configuration, the duty cycle and the basic frequency of operation depend mainly on the capabilities of the individual devices. When the free running or "closed" ring configuration is employed, no more than 21 devices shall be contained in any single ring. Where the "open" ring configuration is employed, the time duration between inputs from the external source shall be no greater than 20 times the propagation delay of the device as specified in the detail specification. While this test condition affords the opportunity to continuously monitor the test for catastrophic failures (i.e. ring stoppage), this shall not be considered acceptable as a substitute for the intermediate measurements (see 3.2).

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Device history, whether screened or unscreened (see 3.1).
(b) Test temperature (case or ambient). Unless otherwise specified, the test temperature shall be the maximum rated operating temperature of the device being tested.
(c) Test duration if other than the specified minimums (see 3.1).
(d) Test mounting if other than that specified (see 3).
(e) Test condition (see 3.4).
(f) End point measurements (see 3.2).
(g) Intermediate measurements (see 3.2).
(h) Criteria for failure for end point and intermediate measurements (see 3.2) if other than device specification limits.
(i) Test sample (see 3.3).
(j) Requirements for inputs, outputs, biases, and power dissipation, as applicable (see 3.4).

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METHOD 1005 - Continued

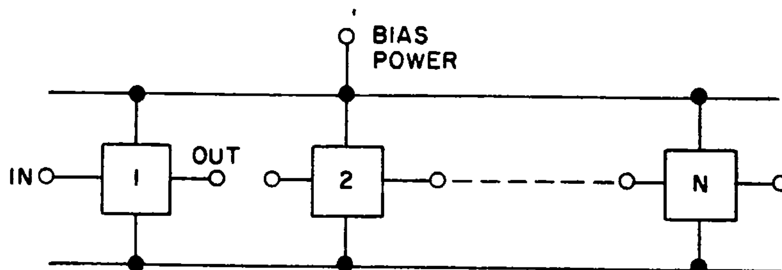


FIGURE 1005-1. Steady state.

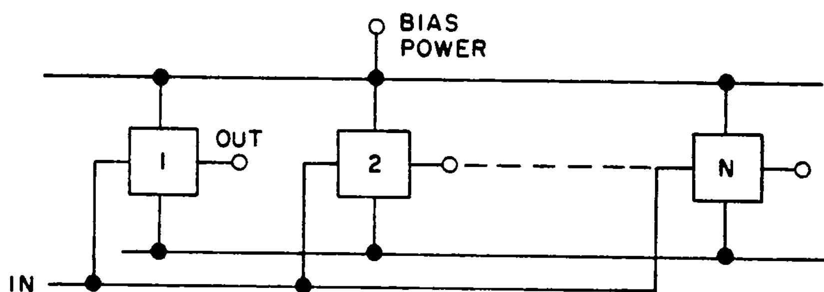
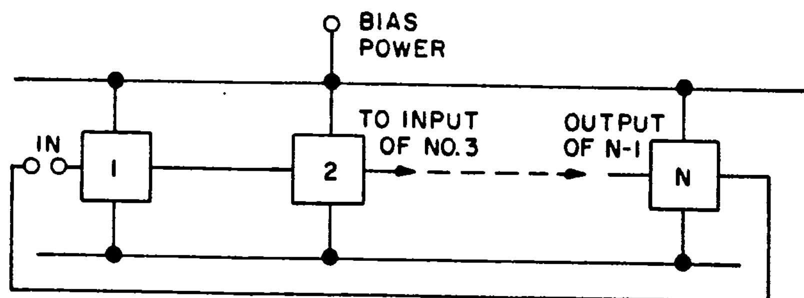


FIGURE 1005-2. Parallel excitation.



NOTE:
1. For free running counter, N is an odd number and the output of N is connected to the input of 1.

FIGURE 1005-3. Ring oscillator.

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METHOD 1006

INTERMITTENT LIFE

1. PURPOSE. The intermittent life test is performed for the purpose of determining a representative failure rate for microelectronic devices or demonstrating quality or reliability of devices subjected to the specified conditions. It is intended for applications where the devices are exposed to cyclic variations in electrical stresses between the "on" and "off" condition and resultant cyclic variations in device and case temperatures.

2. APPARATUS. See method 1005 of this standard.

3. PROCEDURE. The device shall be tested in accordance with all the requirements of method 1005 except that all electrical stresses shall be alternately applied and removed. The "on" and "off" periods shall be inititated by sudden, not gradual, application or removal of the specified electrical inputs (including signal and bias).

4. SUMMARY. In addition to the requirements of method 1005 of this standard, the following detail shall be specified in the applicable procurement document:

(a) Frequency and duration of "on" and "off" cycles.

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METHOD 1007

AGREE LIFE

1. PURPOSE. The purpose of this test is to determine a representative failure rate for microelectronic devices or to demonstrate quality or reliability of devices subjected to the specified conditions where test conditions include a combination of temperature cycling, on-off electrical stressing and vibration to simulate as closely as possible actual system applications and environments.

2. APPARATUS. The apparatus required shall be as described in method 1005 of this standard except that the temperature chambers shall be capable of following the specified test profile of figures 1 or 2 of MIL-STD-781 and suitable equipment shall be provided to satisfy the requirements for vibration as specified.

3. PROCEDURE. This test shall be conducted in accordance with all the requirements of method 1005 of this standard with the exceptions that temperature shall be cycled, periodic vibration shall be applied, and electrical stresses shall be applied in on-off cycles where and as required in the specified test level of MIL-STD-781. Only test levels E, F, G, H and J of MIL-STD-781 shall be considered acceptable as test conditions. Selection of the temperature range should take into account the temperature rise associated with the devices under test.

Test conditions for method 1007	Test level per MIL-STD-781	Temperature range °C
A	E	-54 to +55
B	F	-54 to +71
C	G	-54 to +95
D	H	-65 to +71
E	J	-54 to +125
F	Test level F with modified low temp.	0 to +70

4. SUMMARY. In addition to the requirements of method 1005 of this standard, the following details shall be specified in the applicable procurement document:

(a) Test condition (see 3).
(b) Test profile, specify figure 1 or 2 of MIL-STD-781 and specify on-time and transfer-times, as applicable.
(c) Total on-time.

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METHOD 1008

HIGH-TEMPERATURE STORAGE

1. PURPOSE. The purpose of this test is to determine the effect on microelectronic devices of storage at elevated temperatures without electrical stress applied. This method may also be used in a screening sequence or as a preconditioning treatment prior to the conduct of other tests. This test shall not be used to determine device failure rates for other than storage conditions.

2. APPARATUS. The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the specified temperature and suitable electrical equipment to make the specified end point measurements.

3. PROCEDURE. The device shall be stored at the specified ambient condition for the specified time. End point measurements shall be made at 0 hours and at the specified final end point (duration of test in hours) $^{+72}_{-0}$ hours. End point measurements shall be made at standard test conditions and sample units shall be removed from the test ambient and allowed to reach standard conditions before final end point measurements. Additional measurements may be made at intermediate points. It may be desirable to make end point and, where applicable, intermediate measurements on a serialized device basis or on the basis of a histogram distribution by total sample in order to increase the sensitivity of the test to parameter degradation or the progression of specific failure mechanisms with time and temperature.

3.1 Test condition. The ambient (see 4(a)) test temperature shall be specified in accordance with the following test conditions:

Test condition	Temperature
A	75°C
B	125°C
C	150°C
D	200°C
E	250°C
F	300°C
G	400°C
H	500°C

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition letter (see 3.1).
(b) Test duration (see 3.).
(c) End point measurements (see 3).
(d) Intermediate measurements, if applicable (see 3).
(e) Device serialization or special data reporting requirements (see 3).

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METHOD 1009

SALT ATMOSPHERE (CORROSION)

1. PURPOSE. This test is proposed as an accelerated laboratory corrosion test simulating the effects of seacoast atmospheres on devices.

2. APPARATUS. Apparatus used in the salt-atmosphere test shall include the following:

(a) Exposure chamber with racks for supporting devices.
(b) Salt-solution reservoir.
(c) Means for atomizing the salt solution, including suitable nozzles and compressed-air supply.
(d) Chamber-heating means and controls.
(e) Means for humidifing the air at a temperature above the chamber temperature.

3. PROCEDURE. The device shall be placed within the test chamber. A salt atmosphere fog having a temperature of 35°C (95°F) shall be passed through the chamber for the specified test duration (see test conditions below), unless otherwise specified. The fog concentration and velocity shall be so adjusted that the rate of salt deposit in the test area is between 10,000 and 50,000 $mgm/m^2/day$. When this test is performed as part of a group or subgroup of tests where lead integrity tests in accordance with method 2004, test conditions B1 and C1 are conducted prior to exposure to this test, the initial conditioning (see 3.1) may be omitted. When a group or subgroup of tests is performed which includes testing in accordance with more than a single test method where the initial conditioning requirements (see 3.1) are imposed, the conditioning shall be applied only once prior to the performance of these methods and shall be omitted from the succeeding test method(s).

3.1 Initial conditioning. Prior to mounting specimens for the salt atmosphere test, the device leads shall be subjected to bending and torsion stresses. Each lead of each specimen shall be exposed to the following stresses:

(a) Lead bend. A force of 8.0 ± 1.0 ounce, unless otherwise specified, shall be applied to the lead at a distance of 0.12 ± 0.03 inch from the device body or at the end of the lead if it is shorter than 0.12 inch. The force shall be applied to each lead once in each of two mutually perpendicular directions, both directions being perpendicular to the original lead position. When devices have leads which are formed close to the body, the forces may be applied 0.12 ± 0.03 inch from the form. Bending force shall be applied in accordance with the applicable diagram of figure 2004-1, method 2004, of this standard. For a device lead which bends noticeably when less than the specified force is applied, the bend shall be continued until the specified force is achieved or until the bend equals 90^{+10}_{-0}°, whichever condition occurs first. The lead shall then be restored to its original position. For ribbon lead flat packs (such as the TO-84 and TO-89 packages) where the lead cross section is 0.002 x 0.020 inches or less and the width to thickness ratio is greater than 8 to 1, a force of 3 ± 0.3 ounces shall be applied instead of the 8 ounce force specified above and the lead bend conditioning shall not be applied to the end leads of packages (such as the TO-89 package) where the application of the bending stress will apply primarily torsion at the lead seal.

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METHOD 1009 - Continued

(b) Lead torsion. A torque of 2.0 ± 0.2 oz-in., unless otherwise specified, shall be applied to the lead at a distance of 0.12 ± 0.03 inch from the device body or at the end of the lead if it is shorter than 0.12 inch. The torque shall be applied about the axis of the lead once in each direction (clockwise and counterclockwise). When devices have leads which are formed close to the body, the torque may be applied 0.12 ± 0.03 inch from the form. Torque shall be applied in accordance with the applicable diagram of figure 2004-2, method 2004 of this standard. For device leads which twist noticeably when less than the specified torque is applied, the twist shall be continued until the specified torque is achieved or until the twist equals $30^\circ {}^{+10^\circ}_{-0^\circ}$ whichever condition occurs first. The lead shall then be restored to its original position.

3.2 Length of test. The length of salt atmosphere test shall be that indicated in one of the following test conditions, as specified:

Test condition	Length of test
A - - - - - -	24 hours
B - - - - - -	48 hours
C - - - - - -	96 hours
D - - - - - -	240 hours

3.3 Examination. Upon completion of the test, and to aid in the examinations, devices shall be prepared in the following manner, unless otherwise specified: Salt deposits shall be removed by a gentle wash or dip in running water not warmer than 100° F (37.8° C) and a light brushing, using a soft-hair brush or plastic bristle brush. A device with illegible markings, evidence (when examined with magnification of between 5X and 10X) of flaking or pitting of the finish, or corrosion that will interfere with the application of the device shall be considered a failure. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition (see 3.2). Unless otherwise specified, test condition A shall apply.
(b) Measurements and examinations after test (see 3.3).

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METHOD 1010

TEMPERATURE CYCLING

1. PURPOSE. This test is conducted for the purpose of determining the resistance of a part to exposures at extremes of high and low temperatures, and to the effect of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. These conditions may also be encountered in equipment operated noncontinuous in low-temperature areas or during transportations. Permanent changes in operating characteristics and physical damage produced during thermal shock result principally from variations in dimensions and other physical properties. Effects of temperature cycling include cracking and delamination of finishes. cracking and crazing of embedding and encapsulating compounds, opening of thermal seals and case seams, leakage of filling materials, and changes in electrical characteristics due to mechanical displacement or rupture of conductors or of insulating materials.

2. APPARATUS. Suitable chamber(s) shall be used for the extreme temperature conditions of steps 1 and 3. The air temperature of the chamber(s) shall be held at each of the extreme temperatures by means of circulation and sufficient hot- or cold-chamber thermal capacity so that the ambient temperature shall reach the specified temperature within 2 minutes after the specimens have been transferred to the appropriate chamber.

3. PROCEDURE. Specimens shall be placed in such a position with respect to the airstream that there is substantially no obstruction to the flow of air across and around the specimen. When special mounting is required. it shall be specified. The specimen shall then be subjected to the specified condition for the specified number of cycles performed continuously. One cycle consists of steps 1 through 4 of the applicable test condition with the duration of exposure at each temperature as indicated in the table of test conditions. Specimens shall not be subjected to forced circulating air while being transferred from one chamber to another where applicable. Whether single or multiple chambers are used the effective total transfer time from the specified low temperature to the specified high temperature. or the reverse, shall not exceed 5 minutes. Direct heat conduction to the specimen should be minimized.

3.1 Measurements. Specified measurements shall be made prior to the first cycle and upon completion of the final cycle. Unless otherwise specified, these measurements shall include all device electrical parameters specified in the applicable procurement document, and an external visual examination for evidence of damage and legibility of markings and a test for hermeticity (seal) or package integrity. Where this test is performed as part of a group or subgroup of test, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

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METHOD 1010 - Continued

Temperature-cycling test conditions

Step	Minutes	Test condition A Temperature	Test condition B Temperature	Test condition C Temperature	Test condition D Temperature	Test condition E Temperature	Test condition F Temperature
		°C	°C	°C	°C	°C	°C
1	10 min	-55^{+0}_{-3}	-55^{+0}_{-5}	-65^{+0}_{-5}	-65^{+0}_{-5}	-65^{+0}_{-5}	-65^{+0}_{-5}
2	5 max	25^{+10}_{-5}	25^{+10}_{-5}	25^{+10}_{-5}	25^{+10}_{-5}	25^{+10}_{-5}	25^{+10}_{-5}
3	10 min	85^{+3}_{-0}	125^{+3}_{-0}	150^{+5}_{-0}	200^{+5}_{-0}	350^{+5}_{-0}	500^{+5}_{-0}
4	5 max	25^{+10}_{-5}	25^{+10}_{-5}	25^{+10}_{-5}	25^{+10}_{-5}	25^{+10}_{-5}	25^{+10}_{-5}

NOTE: The time at the high and low temperatures shall be sufficient to stabilize the devices under test at the specified temperature and if carriers or holders employed or other factors make 10 minutes inadequate for stabilization, the time at the temperature extremes shall be increased to meet this requirement.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Special mounting, if applicable (see 3).
(b) Test-condition letter (see 3).
(c) Number of test cycles (see 3). Unless otherwise specified, this test shall be conducted for a minimum of 10 cycles.
(d) Measurements before and after cycling (see 3.1).

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METHOD 1011

THERMAL SHOCK

1. PURPOSE. The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. These conditions may be encountered in equipment operated intermittently in low temperature areas. Permanent changes in operating characteristics and physical damage produced during temperature shock result principally from variations in dimensions and other physical properties. Effects of thermal shock include cracking and delamination of substrates or wafers, opening of terminal seals and case seams, and changes in electrical characteristics due to moisture effects or to mechanical displacement of conductors or insulating materials.

2. APPARATUS. The apparatus for this test shall consist of suitable temperature controlled baths containing liquids chosen to obtain the temperature excursion specified in the table of test conditions (see 3) and within the indicated tolerances. It is essential that the baths be placed within close proximity to effect the rapid transfer time specified.

3. PROCEDURE. The device shall be preconditioned by being immersed and in intimate contact with a suitable liquid at the temperature specified in step 1 of the specified test condition for a minimum of 5 minutes. Immediately upon conclusion of the preconditioning time, the device shall be transferred to a liquid at the temperature specified in step 2 of the specified test condition. The device shall remain at the low temperature for a minimum of 5 minutes and then be transferred to a liquid at the step 1 temperature. The device shall remain at the high temperature for a minimum of 5 minutes. Transfer time from high temperature to low temperature and from low temperature to high temperature shall be less than 10 seconds. Unless otherwise specified, the duration of the test shall be 15 complete cycles, where one cycle consists of proceeding from step 1 to step 2 and back to the beginning of step 1. At the conclusion of the specified number of test cycles the device shall be subjected to external visual inspection at a magnification between 10X and 20X for evidence of physical damage to case, leads or seals and then the specified end point measurements shall be made (see 4). (Unless otherwise specified, fine and gross leak tests shall be conducted as end point measurements in addition to the electrical measurements specified.)

Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

Thermal shock test conditions

Test condition	A	B	C	D	E	F
	Temperature	Temperature	Temperature	Temperature	Temperature	Temperature
	°C	°C	°C	°C	°C	°C
Step 1	100^{+5}_{-0}	125^{+5}_{-0}	150^{+5}_{-0}	200^{+5}_{-0}	150^{+5}_{-0}	200^{+5}_{-0}
Step 2	-0^{+0}_{-5}	-55^{+0}_{-5}	-65^{+0}_{-5}	-65^{+0}_{-5}	-195^{+5}_{-5}	-195^{+5}_{-5}

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition (see 3).
(b) Number of cycles, if other than 15 (see 3).
(c) End point measurements (see 3).

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METHOD 1012

THERMAL CHARACTERISTICS

1. PURPOSE. The purpose of this test is to determine the case or junction temperatures (T_C or T_J), heat sink temperature (T_S), thermal response time, or the thermal resistance (θ_{J-C} or θ_{J-A}) of microelectronic devices.

1.1 Definitions. The following definitions and symbols shall apply for the purpose of this test:

(a) Thermal resistance, junction to ambient (θ_{J-A}) in degrees centigrade per watt.
(b) Thermal resistance, junction to case (θ_{J-C}) in degrees centigrade per watt.
(c) Junction temperature (T_J), in degrees centigrade.
(d) Case temperature (T_C), in degrees centigrade.
(e) Heat sink temperature (T_S), in degrees centigrade. For devices which, in their normal application are intimately connected (by pressure contact, adhesive, soldering, welding or other means) to a heat sink, the heat sink temperature as measured at a point on the heat sink nearest to the device will be taken as the effective heat sink temperature (T_S), and this temperature may also be used as the equivalent case temperature (T_C).
(f) Ambient temperature (T_A), in degrees centigrade . The ambient temperature will be monitored by 3 thermal probes and an average of the 3 used. The ambient thermal probes will be positioned in close proximity to the component being measured and when in an air environment, they should have a low absorptivity to reduce radiation effects. During ambient temperature recording, the ambient medium will have velocities not exceeding those set up by natural means except in specific forced air ventilation tests.
(g) Thermal time constant (T_{CX}), is the time required for the junction temperature within a device to reach 63.2 percent of the final value of junction temperature change caused by application of a step function in power dissipation when the device case or ambient temperature as specified, is held constant.
(h) Thermal response time (T_R), is the time required for the junction temperature within a device to reach 90 percent of the final value of junction temperature change caused by application of a step function in power dissipation when the device case or ambient temperature, as specified, is held constant.

2. APPARATUS. The apparatus required for these tests shall include the following as applicable to the specified test condition letter:

(a) Thermocouple material shall be copper/constantan for the temperature range - 190° to 350°C. The wire size shall be no larger than AWG size 30. The junction thermocouple shall be welded together to form a bead rather than soldered or twisted. The accuracy of the thermocouple shall be ±1.0°C where devices are exposed to convection cooling and ±2.0°C for forced air ventilation.
(b) Infrared microradiometer capable of measuring radiation in the 2 to 10 micron range and having sufficient resolution to detect radiation emitted from an area 1.5 by 1.5 mils.
(c) Controlled temperature chamber capable of maintaining the specified ambient temperature with indicator or a controlled temperature heat sink capable of maintaining the specified heat sink temperature.
(d) Suitable electrical equipment as required to provide controlled levels of conditioning power and to make the specified measurements.

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METHOD 1012 - Continued

3. PROCEDURE.

3.1 Test condition A. Case temperature (T_C).

3.1.1 Hex-base mounted devices. A small hole, just large enough to insert the thermocouple, shall be drilled approximately 1/32 inch deep into the flat of the case hex at a point chosen by the manufacturer. The edge of the hole should then be peened with a small center punch to force a rigid mechanical contact with the welded bead of the thermocouple. If forced air ventilation is used, the thermocouple shall be mounted away from the air stream and the thermocouple leads close to the junction shall be shielded.

3.1.2 Other devices. Other types of devices will be mounted by their normal mounting means in their normal mounting position. A thermocouple shall be attached as near as is possible to the center of the bottom of the device case directly under the chip or substrate. As an alternative, a microradiometer scan may be made at the same point on the bottom of the case, in which case the surface emissivity must be known and controlled. The test specimen shall be operated at the specified power level and the following data recorded:

(a) Specimen case temperature (T_C) or heat sink temperature (T_S), where applicable.
(b) Ambient temperature (T_A).
(c) Power dissipated (P_D).

The specimen shall be considered stabilized when the measured case temperature does not change by more than 2°C per hour.

3.2 Test condition B. Junction temperature (T_J). The junction temperature of semiconductor devices cannot be measured directly except by the infrared microradiometer method. With the specimen in its normal mounting position and specified power applied, the radiometer shall be focused on the junction to be measured. The top cap or lid shall be removed or opened sufficiently to permit observation of the active chip or substrate. The opened area shall be covered with a material exhibiting high transmissibility in the IR range to eliminate convection currents. The surface emissivity must be known and controlled. The following data shall be recorded after the device is stabilized:

(a) Case temperature (T_C).
(b) Junction temperature (T_J).
(c) Power dissipated (Pd).
(d) Ambient temperature (T_A).
(e) Heat sink temperature (T_S).
(f) Ambient fluid.

The specimen shall be considered stabilized when measured temperature does not change by more than 2°C per hour.

3.3 Test condition C. Thermal resistance (θ_{J-C}). The thermal resistance of a microelectronic device may be calculated from a knowledge of the case and junction temperature and the power dissipation in the device being measured or may be determined by measurement of a temperature sensitive parameter of a semiconductor junction(s) within the device. The latter method involves variation of ambient temperature and power dissipation within the device and avoids the necessity of performing a direct measurement of device junction temperature. The thermal resistance of a microelectronic device may be determined by performing any of the procedures described in 3.3.1 to 3.3.6. Test condition C_1 provides for the calculation of θ_{J-C} from case and junction temperatures and power dissipation. Test condition C_2 describes a diode (two terminal) measurement to determine θ_{J-C}. Test conditions C_3 through C_6 describe transistor (three terminal) measurements to determine θ_{J-C}. Unless otherwise specified, where more than one diode junction or transistor in the device is available through the external leads (or by probing, for unsealed devices), that available junction or transistor which dissipates the greatest amount of power in the particular

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METHOD 1012 - Continued

device shall be selected for θ_{J-C} measurements. Where thermal resistance from junction to ambient is being measured, substitute θ_{J-A} for θ_{J-C} in the test condition C procedures.

3.3.1 Test condition C_1. Thermal resistance (θ_{J-C}). Where the junction temperature (T_J), case temperature (T_C), and power dissipation (P_D) for the same junction and under the same conditions are specified or have been measured using test conditions A and B of this method, the thermal resistance (θ_{J-C}) may be determined as follows:

$$\theta_{J-C} = \frac{T_J - T_C}{P_D}$$

Where: P_D = Power dissipation, watts

3.3.2 Test condition C_2. θ_{J-C} (Diodes). This test shall be done in accordance with figure 1012-1. S_1 is closed for a much longer interval (heat) than it is opened (measurement). The measurement interval should be short compared to the thermal response time of the device being measured. The constant measurement current is a small current (of the order of a few milliamperes) and so selected that the magnitude of V_{F_1} changes appropriately with the device material (silicon approximately 2mv/°C) and junction temperature. The heating current source is adjustable.

The measurement is made in the following manner. The case ambient or other reference point is elevated to a high temperature, T_2, not exceeding the maximum junction temperature and the forward voltage drop V_{F_1} read with the heating source supplying no current (i.e., the forward voltage V_{F_1} is to be read at the start of the measurement interval). An oscilloscope makes a convenient detector. At T_2 there will be a small power dissipated in the device due to the measurement current source. The reference is then reduced to a lower temperature T_1, and power P_D is applied to heat the device by increasing the current from the constant current source until the same value of V_{F_1} is read as was read above. However, if P_D is calculated as the heating power contributed by the heating current source, only the equation:

$$\theta_{J-C} = \frac{T_2 - T_1}{P_D} \quad \text{gives } \theta_{J-C} \text{ accurately}$$

Where: $P_D = V_{F_1} \; I_{F_1}$

3.3.3 Test condition C_3. θ_{J-C}, Forward voltage drop, emitter to base. This test shall be done in accordance with figure 1012-2. S_1 is closed for a much larger interval (heat) than it is open (measurement). The measurement interval should be short compared to the thermal response time of the device being measured. The constant measurement current is a small current (of the order of a few milliamperes) so selected that the magnitude of V_{EB} changes approximately 2 mv/°C of junction temperature change. The heating current source is adjustable. This procedure is recommended for devices having relatively short thermal response times.

The measurement is made in the following manner: The case, ambient or other reference point is elevated to a high temperature T_2, not exceeding the maximum junction temperature, and the emitter to base voltage V_{EB} read with the constant current source supplying no current. V_{EB} is to be read at the start of the measurement interval. An oscilloscope makes a convenient detector. At T_2 there will be a small power dissipated in the device due to the measurement current source. The reference temperature is then reduced to a lower temperature T_1, and power P_D, is applied to heat the device;

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METHOD 1012 - Continued

by increasing the current from the constant current source, until the same value of V_{EB} is read as was read above. However, if P_D is calculated as the heating power contributed by the heating current source, only the equation

$$\theta_{J-C} = \frac{T_2 - T_1}{P_D} \text{ gives } \theta_{J-C} \text{ accurately.}$$

Where:

$$P_D = (n) (I_C V_{CB} + I_E V_{EB})$$

$$n = \text{duty cycle}, \left[\frac{t_{on}}{t_{total}} \right]$$

3.3.4 Test condition C_4. θ_{J-C}, Forward voltage drop, emitter to base (continuous). This test shall be done in accordance with figure 1012-3. The measurement technique assumes that the forward emitter voltage drop varies with temperature. It further assumes that during the course of measurement, the variation in forward emitter voltage drop varies monotonically due to temperature and is much greater than that due to the variation with collector voltage. These assumptions must be maintained to achieve valid and reproducible results.

The measurement is made in the following manner. The case, ambient, or other reference point is elevated to a high temperature T_2, not exceeding the maximum junction temperature. Current I_C is set to a value and a voltage V_2 applied to the collector base diode. The value of V_2 applied shall be low yet high enough so that the device is operating in a normal manner. V_{EB} is read under these conditions. The reference temperature is reduced to a lower temperature T_1 and V_{CC} varied until the same value of V_{EB} is read as was read above. The thermal resistance is then:

$$\theta_{J-C} = \frac{T_2 - T_1}{I_C (V_1 - V_2)}$$

where V_1 is the collector-base voltage V_{CB} applied at temperature T_1, and V_2 is V_{CB} at temperature T_2.

3.3.5 Test condition C_5. θ_{J-C}, Forward voltage drop, collector to base. This test shall be done in accordance with figure 1012-4. Switches S_1 and S_2 are ganged switches and are so arranged that S_2 opens very shortly after S_1 opens and such that the delay between the openings is much shorter than the thermal response time of the device being measured. S_1 and S_2 should be closed (heat interval) for a much larger time than they are open (measurement interval) and the measurement interval should be short (less than 1/10 T_R) compared to the thermal response time of the device being measured. This procedure is recommended for devices having relatively long thermal response times.

The measurement is made in the following manner: The case, ambient or other reference point is elevated to a high temperature T_2, not exceeding the maximum junction temperature, and the collector-base voltage, V_{CB} is read. This reading is made at the beginning of the measurement interval. An oscilloscope makes a convenient detector. The reference temperature is then reduced to a lower temperature, T_1. The heating power, P_D, is adjusted by adjusting the heating current source in the emitter circuit until the same value of V_{CB} is read as was read above. The θ_{J-C} is calculated from the equation

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$$\theta_{J\text{-}C} = \frac{T_2 - T_1}{P_D}$$

Where: $P_D = (n)\,(I_C\,V_{CB} + I_E\,V_{EB})$

n = duty cycle $\left[\frac{t_{on}}{t_{total}}\right]$

3.3.6 Test condition C_6. $\theta_{J\text{-}C}$, DC current gain (continuous). This test shall be done in accordance with figure 1012-5. The measurement technique assumes that the current gain varies with temperature. The rate of change is unimportant. It further assumes that during the course of measurement the variation in current gain varies monotonically due to temperature variation and is much greater than that due to the variation with collector voltage. These assumptions must be maintained to achieve valid and reproducible results.

The measurement is made in the following manner. The case, ambient, or other reference point is elevated to a high temperature T_2, not exceeding the maximum junction temperature. Current I_C is set to a value and a voltage applied to the collector base diode V_2. The value of V_2 applied shall be low yet high enough so that the device is operating in a normal manner. I_B is read under these conditions. The reference temperature is reduced to a lower temperature T_1 and V_{CC} is varied until the same value of I_C is read as was read above. The thermal resistance is then:

$$\theta_{J\text{-}C} = \frac{T_2 - T_1}{I_C\,(V_1 - V_2)}$$

Where: V_1 is the collector voltage V_{CB} applied at temperature, T_1 and V_2 is V_{CB} at temperature T_2.

3.4 Test condition D. Junction temperature (T_J). Where the internal thermal resistance ($\theta_{J\text{-}C}$) of a microelectronic device is specified or has been measured in accordance with test conditions C_2 through C_5 of this method and where the case temperature (T_C) and power dissipation (P_D) are specified or measured for the same junction in the device and under the same conditions, the junction temperature (T_J) may be determined as follows:

$$T_J = T_C + (\theta_{J\text{-}C})\,(P_D)$$

Where: P_D = Power dissipation, watts

3.5 Test condition E. Thermal time constant and response time. When a step function of power dissipation is applied to a semiconductor device, the junction temperature does not rise as a step function, but rather as a complex exponential curve. The change in junction temperature as a function of time resulting from the sudden application, increase or removal of power dissipation in the junction shall be observed using an IR radiometer with a response time of less than 1 millisecond or electrical equipment with a response time of less than 1 millisecond and sufficient sentitivity to read a precalibrated temperature sensitive electrical parameter of the junction. During this test the device case or ambient temperature, as specified, shall be held constant, the step function of power dissipation shall be applied and the waveform of the junction temperature response versus time shall be recorded from the time of application to the time when the junction temperature reaches a stable value as evidenced by a temperature change of less than 2°C per hour.

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3.5.1 Thermal time constant. The value of thermal time constant (T_{CX}) for the device under specified conditions shall be determined as the time required in milliseconds after application of the step function in power for the junction temperature to reach 63.2 percent of the final stable value.

3.5.2 Thermal response time. The value of thermal response time (T_R) for the device under specified conditions shall be determined as the time required in milliseconds after application of the step function in power for the junction temperature to reach 90 percent of the final stable value.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Test condition letter (see 3).
(b) Mounting arrangement for device under test.
(c) Test temperature(s) (case, ambient, sink or junction temperatures), as applicable.
(d) Test voltage, test currents and power dissipation where applicable including duty cycle for pulse test.
(e) θ_{J-C} (or θ_{J-A}), T_{CX} or T_R, as applicable, for tests to determine compliance with specified values of these parameters.

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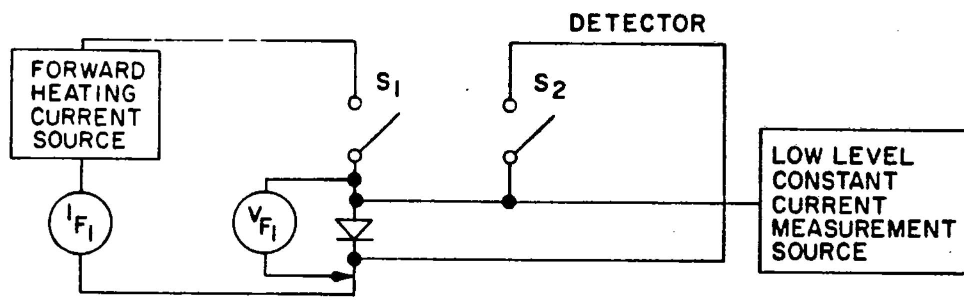

FIGURE 1012-1

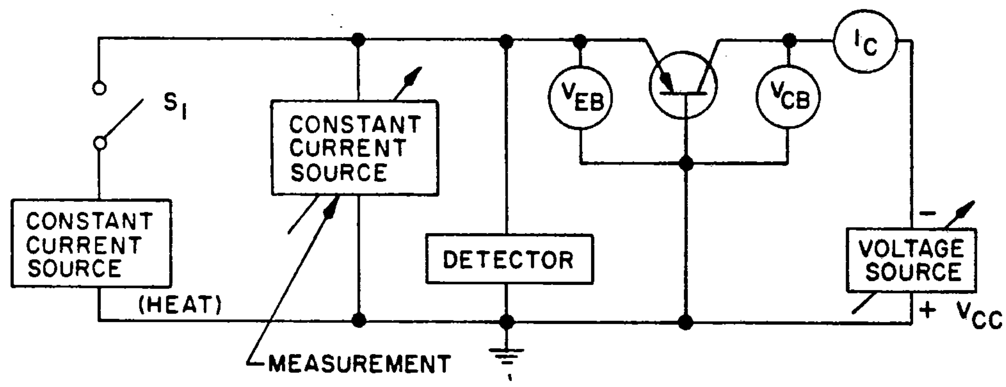

FIGURE 1012-2

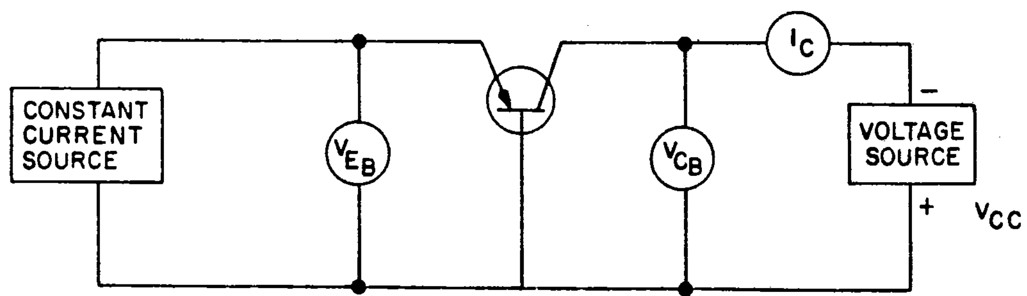

FIGURE 1012-3

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METHOD 1012 - Continued

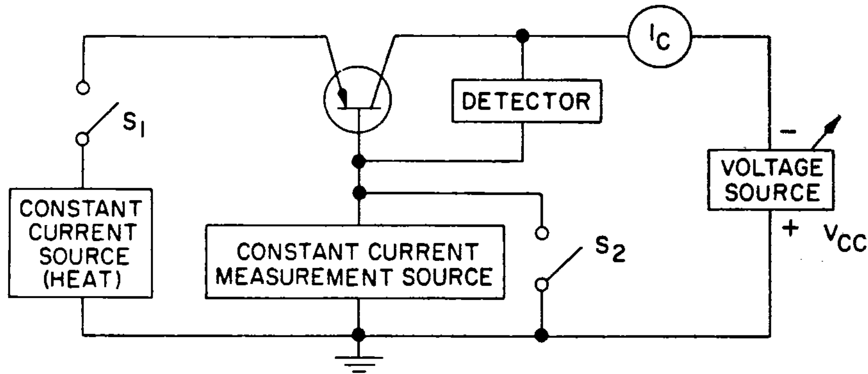

FIGURE 1012-4

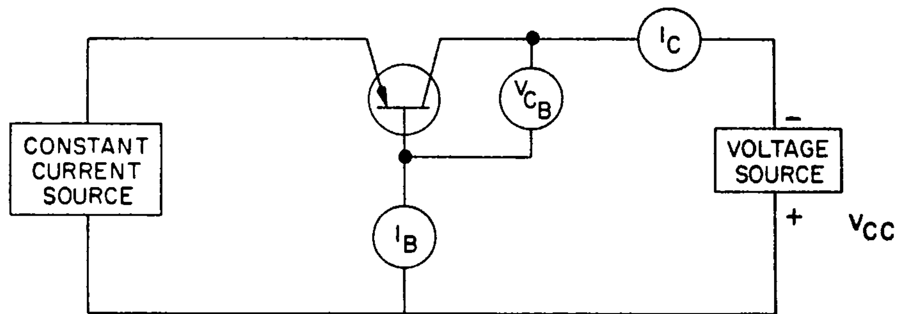

FIGURE 1012-5

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METHOD 1013

DEW POINT

1. PURPOSE. The purpose of this test is to detect the presence of moisture trapped inside the microelectronic device package in sufficient quantity to adversely affect device parameters. The most sensitive indicator of moisture is device leakage current. This test specifies a lower temperature of -65°C for the normal dew point test. It may be desirable in some cases, where the presence of moisture in concentrations lower than that would be revealed at this lower temperature, to extend the lower temperature downward.

2. APPARATUS. The apparatus used in this test shall be capable of varying the temperature from the specified high temperature to -65°C while the parameter is being measured.

3. PROCEDURE. The voltage and current specified in the applicable procurement document shall be applied to the terminals and the device leakage current or other specified parameter(s) continuously monitored from the specified high temperature to -65°C and back to the high temperature. The dew point temperature is indicated by a sharp discontinuity in the parameter being measured with respect to temperature. If no discontinuity is observed, it shall be assumed that the dew point is at a temperature lower than -65°C and the device being tested is acceptable. Devices which demonstrate instability of the measured parameter at any point during this test shall be rejected even though a true dew point is not identified. If a high temperature is not specified in the applicable procurement document, the device shall be taken to a temperature at least 10°C above ambient temperature to initiate this test and enable detection of dew point in devices which may already be at saturation. The rate of change of temperature for this test shall be no greater than 10°C per minute. The test voltage shall be at least equal to the rated breakdown voltage of the device since it is necessary to apply sufficient voltage to achieve ionization.

4. SUMMARY. The following details shall be specified on the applicable procurement document:

(a) Test temperature, high (see 3) and low if other than -65°C (see 1).
(b) Test voltage and current (see 3).
(c) Test parameter (see 1 and 3).

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METHOD 1014

SEAL

1. PURPOSE. The purpose of this test is to determine the effectiveness (or the hermeticity) of the seal of microelectronic devices with internal cavities which are evacuated or which contain air or gas. This test is intended to determine those devices which, when exposed for long periods to atmospheres containing high concentrations of water vapor or other gaseous contaminants, would degrade in performance and become latent failures.

1.1 Definitions.

(a) Calculated leak rate. The calculated leak rate is defined as that quantity of dry air at 25°C in atmosphere cubic centimeters flowing through a leak per second when the high-pressure side is at 1 atmosphere (760 mm Hg absolute) and low-pressure side is at a pressure of not greater than 1 mm Hg absolute. True leak rate shall be expressed in units of atmosphere cubic centimeters per second (atm. cc/sec).

(b) Measured leak rate. Measured leak rate is defined as the leak rate of a device as measured under specified conditions and employing a specified test fluid. Measured leak rate shall be expressed in units of atmosphere cubic centimeters per second (atm. cc/sec). For the purpose of comparison, measured leak rates must be converted to calculated leak rates by employing the appropriate formulas (see 3.1).

2. APPARATUS. The apparatus required for the seal test shall be as follows for the applicable test conditions:

2.1 Test condition A. Tracer gas (He) fine leak. Apparatus for this test shall consist of suitable pressure and vacuum chambers and pumps and a mass spectrometer type leak detector preset to read the helium tracer gas, properly calibrated and with a leak rate sensitivity sufficient to read measured helium leak rates of 10^{-9} atm. cc/sec and greater. The volume of the chamber used for leak rate measurement should be held to the minimum practical since this chamber volume has an adverse effect on sensitivity limits. The leak detector indicators shall be calibrated using a diffusion-type leak standard at least once during every working shift.

2.2 Test condition B. Radioisotope fine leak. Apparatus for this test shall consist of:

(a) Radioactive tracer gas activation console.

(b) Counting station consisting of a scintillation crystal, photo-multiplier tube, preamplifier, and ratemeter combination system. The counting station shall be of sufficient sensitivity to determine through the device wall the radiation level of any krypton-85 tracer gas present within the device. The counting station shall have a minimum sensitivity, in counts per minute, corresponding to a measured leak rate of 1×10^{-9} atm cc of krypton-85 per second.

(c) Tracer gas mixture - krypton-85/dry nitrogen. The specific activity of the krypton-85/dry nitrogen mixture shall be a known and predetermined value (determined prior to performing the test) which shall be no less than 100 microcuries per atmosphere cubic centimeter.

2.3 Test condition C. Fluorocarbon gross leak. The apparatus required includes a suitable vacuum/pressure container for the evacuation and subsequent pressure bombing of devices up to 90 psig for 3 hours, a pyrex glass observation dish with a stainless steel mesh located a minimum of 1/4 inch from the bottom of the dish and with provisions to maintain the indicator fluid contained in this dish at a temperature of 125°C, Whatman #50, or equivalent filter paper, magnifier (3X minimum) or stereo zoom microscope arranged for observation of bubbles emanating from devices when

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METHOD 1014 - Continued

immersed in the indicator fluid, 125°C bath, sources of FC-78 and FC-43 or equivalent fluorocarbon liquids, and suitable calibrated instruments to indicate that test temperatures, pressures and times are as specified.

2.4 Test condition D. Penetrant dye gross leak. The following apparatus shall be used for this test:

(a) Pressure chamber capable of maintaining 100 psig for a minimum of 2 hours and of sufficient volume to allow the devices to be covered with solution.
(b) Solution of fluorescent dye (such as Rhodamine B or fluorescein) to which a minimum of 20% and a maximum of 25% by volume of a non-ionic wetting agent has been added.

3. PROCEDURE. Seal tests shall be conducted in accordance with the requirements and procedure of the specified test condition. In all cases where both fine leak (test conditions A and B) and gross leak (test conditions C and D) are conducted, the fine leak test shall be done prior to the gross leak test. Where specified (see 4), measurements after test shall be conducted following the leak test procedures.

3.1 Test condition A. Tracer gas (He) fine leak. The device, in its completed state, shall be placed in a sealed chamber which is pressurized with a tracer gas of 100^{+0}_{-5} percent helium for the predetermined time so that the tracer gas is forced into the specimen if there is a defect in its seal. The pressure shall then be relieved and the specimen transferred to another chamber which is connected to the evacuating system and the mass spectrometer type leak detector. Any tracer gas which was previously forced into the specimen will thus be drawn out and indicated by the leak detector as a measured leak rate (R). The measured leak rate (R) shall be converted to a calculated leak rate (L) at the specific test conditions, the minimum exposure pressure (P_E), minimum time of exposure (t_1) to P_E, and maximum dwell time (t_2) between release of pressure and leak detection shall be determined from the following formula by inserting the value of the internal volume of the device package:

$$R = \frac{LP_E}{P_o}\left(\frac{M_A}{M}\right)^{1/2}\left\{1 - e^{-\left[\frac{Lt_1}{VP_o}\left(\frac{M_A}{M}\right)^{1/2}\right]}\right\} e^{-\left[\frac{Lt_2}{VP_o}\left(\frac{M_A}{M}\right)^{1/2}\right]}$$

Where:

- R = The measured leak rate of tracer gas through the leak in atm cc/sec.
- L = The calculated leak rate in atm cc/sec.
- P_E = The pressure of exposure in atmospheres (gauge pressure).
- P_o = The atmospheric pressure in atmospheres.
- M_A = The molecular weight of air.
- M = The molecular weight of the tracer gas.
- t_1 = The time of exposure to P_E, in seconds.
- t_2 = The dwell time between release of pressure and leak detection, in seconds.
- V = The internal volume of the device package cavity in cc.

3.1.1 Test conditions. Unless otherwise specified, P_E shall be 5 atmospheres minimum, t_1 shall be 1 hour minimum, and t_2 shall be a maximum of 30 minutes. Unless otherwise specified, devices with an internal cavity volume of 0.1 cc or less shall be rejected if the measured leak rate exceeds 5×10^{-8} cc/sec or the calculated leak rate under the conditions of test exceeds 5×10^{-7} cc/sec and devices with an internal cavity volume between 0.1 cc and 10 cc shall be rejected if the measured leak rate exceeds 5×10^{-7} cc/sec or the calculated leak rate under the conditions of test exceeds 5×10^{-6} cc/sec.

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METHOD 1014 - Continued

3.2 Test condition B. Radioisotope fine leak.

3.2.1 Calibration procedure. The activation pressure and soak time shall be chosen to satisfy the following equation:

$$(1) \qquad Q_S = \frac{R}{SKT\bar{P}t}$$

The parameters of the equation are defined as follows:

Q_S = The maximum leak rate allowable in atm cc/sec, for the devices to be tested.
R = The internal count, in counts per minute, of the device above the ambient background after activation if the device leak rate were exactly equal to Q_S. This is the reject count above the background of the component.
S = The specific activity, in microcuries per atmosphere cubic centimeter, of the krypton-85 tracer gas in the activation system.
K = The overall counting efficiency of the scintillation crystal in counts per minute per one microcurie of krypton-85 in the internal void of the specific component being evaluated. This factor varies with component configurations, component materials, dimensions of the scintillation crystal and other factors. The counting efficiency shall be determined in accordance with 3.2.2.
T = Soak time, in hours, that the devices are to be activated.
$\bar{P}$ = $P_e^2 - P_i^2$, where P_e is the activation pressure in atmospheres absolute and P_i is the original internal pressure of the devices in atmospheres absolute. The activation pressure (P_e) is established by specification, or if a convenient soak time (T) has been established, the activation pressure (P_e) can be adjusted to satisfy equation (1).
t = Conversion of seconds to hours and is equal to 3,600 seconds per hour.

3.2.2 Determination of counting efficiency (K). The counting efficiency (K) of equation (1) shall be determined as follows:

(a) A representative unit of the device type being tested shall be tubulated and the internal void of the device shall be back-filled through the tubulation with a known volume and known specific activity of krypton-85 tracer gas.
(b) The tubulation shall be pinched off and the device shall be placed in the shielded scintillation crystal that will be used to evaluate the leak rates of the devices.
(c) The counts per minute shall be directly read from the counting station ratemeter and from this value the counting efficiency, in counts per minute per microcurie, shall be calculated.

3.2.3 Testing procedure. The devices shall be placed in a radioactive tracer gas activation tank. The tank shall be evacuated to 0.5 mm Hg. The devices shall be subjected to a minimum of 5 atmospheres absolute pressure of krypton-85/dry nitrogen mixture for a minimum of 12 minutes. (Actual pressure and soak time shall be determined in accordance with 3.2.1.) The krypton-85/dry nitrogen gas mixture shall be evacuated back to storage until 0.5 mm Hg vacuum exists in the activation tank. The activation tank shall then be backfilled with air (air wash). The devices shall then be removed from the activation tank and leak tested within 4 hours after removal with a scintillation-crystal-equipped counting station. The actual leak rate of the component shall be calculated with the following equation:

$$(2) \qquad Q = \frac{(\text{Actual readout in counts per minute}) \times Q_S}{R}$$

Where: Q = actual leak rate in atm cc/sec, and Q_S and R are defined as in 3.2.1.

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METHOD 1014 - Continued

Unless otherwise specified, devices that exhibit a measured leak rate equal to or greater than 5×10^{-8} atmospheres cubic centimeters of krypton-85 per second shall be considered a failure.

3.2.4 Personnel precautions. An Atomic Energy Commission (AEC) license is necessary for possession and use of the krypton-85 leak test equipment. In the use of gas, AEC regulations should be followed and the maximum permissible tolerance levels prescribed by the National Committee on Radiological Protection should be observed.

3.3 Test condition C. Fluorocarbon gross leak. This test shall be conducted in two steps using the procedure and sequence of 3.3.1 and 3.3.2 below. Failure, as evidenced by a single bubble or a stream of bubbles, in either step of the sequence shall constitute failure of the device to pass the gross leak test.

3.3.1 Gross leak step 1. For package leaks $> 10^{-3}$atm/cc/sec. This procedure is designed to identify severe package leaks which though generally observable during external visual examination are nevertheless, frequently missed due to operator fatigue, inattention, or faulty technique. Included in this category are package cracks of all types, solder voids or tilted lids, flange leakers and blow holes in the package or lid sealing materials. The devices subjected to this examination shall be immersed, with the uppermost portion at a minimum depth of 2 inches below the surface of the indicator fluid, lid downward, one at a time (or in such a configuration that a single bubble from a single device out of a group under observation may be clearly observed as to its occurrence and source) in FC-43 maintained at 125 ± 5°C. Leakers will be identified by a bubble or stream of bubbles. The device shall be observed against a dull, non-reflective black background through the magnifier from the instant of immersion until 30 seconds after immersion, or until bubbles occur. Devices which display no bubbles are acceptable. Devices for which a single bubble is observed are considered rejects.

3.3.2 Gross leak step 2. For package leaks $> 10^{-5}$atm/cc/sec. Procedure 2 is designed to overlap procedure 1 as well as the upper limits of the helium fine leak test (10^{-5}atm/cc/sec). Leaks detectable by this procedure but not generally detected by microscopic examination are generally caused by fine package cracks or pores, minute pinholes in solder, minute weld flange pinholes and leaks around metal to glass seals. The device shall be enclosed in the vacuum/pressure vessel and a vacuum (maximum pressure of 1 torr) shall be drawn and retained for 1 hour. After that time, and without breaking vacuum FC-78 shall be drawn into the vacuum/pressure vessel by inserting a hose from the vacuum/pressure vessel into a container of FC-78 and opening a valve in the hose line between the FC-78 and the chamber. For devices with an internal cavity volume of 0.1 cc or less, when the FC-78 has been introduced into the vessel, the pressure in the vessel shall be increased and maintained at 90 psig for a duration of 3 hours minimum. For devices with an internal cavity volume in excess of 0.1 cc, a pressure of 50 psig shall be applied and maintained for a duration of 3 hours minimum. At the end of this time, the pressure shall be removed and the devices shall be extracted from the pressure vessel and be retained in a bath containing the bomb fluid, FC-78. When the devices are removed from the FC-78 they shall be dried for 3 ± 1 minutes in air prior to immersion in the indicator fluid. The devices shall be immersed, with the uppermost portion at a minimum depth of 2 inches below the surface of the indicator fluid, lid downward, one at a time (or in such a configuration that a single bubble from a single device out of a group under observation may be clearly observed as to its occurrences and source), into the leak indicator fluid, FC-43 maintained at 125 ± 5°C. The device shall be observed against a dull, non-reflective black background through the magnifier from the instant of immersion. Leakers will be identified by a bubble or stream of bubbles. Devices which display no bubbles are acceptable. Devices for which a single bubble is observed are considered rejects.

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METHOD 1014 - Continued

3.3.3 Precautions. The following precautions shall be observed in conducting the fluorocarbon gross leak test:

(a) Fluorocarbons FC-43 and FC-78 must be filtered through Whatman #50 or equivalent filter paper prior to use. Bulk filtering and storage is permissable. Liquid which has accumulated observable quantities of particulate matter during use must be discarded or reclaimed by filtration for re-use.
(b) Observation dish must be filled to assure coverage of the device package to a minimum depth of 2 inches.
(c) Illumination must be adjusted to provide maximum visibility at the sample position, and the background behind the glass observation dish should be a dull non-reflective black.
(d) Although the fluorocarbon liquids are inert and their fumes harmless even in significant concentrations, testing should be conducted in a hood or other well-ventilated locations. The observation dish should be covered at all times when not in use to minimize evaporation losses.
(e) When partially fluorinated fluorocarbon fluids are used in place of the FC-78, there are additional risks incurred due to contamination from moisture and dissolved greases and the possibility of damage to the markings or other elements of the device structure.

3.4 Test condition D. Penetrant dye gross leak. This test shall be performed on transparent glass encased devices only and shall not be used on oil or grease-filled devices. The pressure chamber shall be filled with the dye solution to a depth sufficient to completely cover all the devices. The devices shall be placed in the solution. The chamber shall be pressurized to 100 psig minimum for 2 hours minimum. The devices shall then be removed and carefully washed using a cleaner such as acetone or trichloroethylene. This shall be followed by an alcohol rinse and an air-jet dry. The devices shall then be examined under magnification of 7X to 20X power using ultraviolet light as the source of illumination. The source of the ultraviolet light shall have its peak radiation at 3650A and shall be filtered through a medium (usually glass) possessing peak transmission in the region of 3650A and minimal transmission for all other wavelengths. Any evidence of dye penetration into the device shall constitute a failure.

3.5 Retest. Devices which fail gross leak (test condition C or D) test shall not be retested for acceptance under any circumstances. Devices which fail fine leak (test condition A or B) test shall not be retested for acceptance unless specifically permitted by the applicable procurement document. Where fine leak retest is permitted, the entire leak test procedure for the specified test condition shall be repeated. That is, retest consisting of a second observation or leak detection without a re-exposure to the tracer fluid or gas under the specified test condition shall not be permissible under any circumstances.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition letter (see 3).
(b) For test conditions A and B, specify accept or reject leak rate(s), either measured (R) or calculated (L) in atm. cc/sec. (See 3.1.1 and 3.2.3.)
(c) Where applicable, measurements after test (see 3).

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METHOD 1015

BURN-IN SCREEN

1. PURPOSE. The burn-in screen is performed for the purpose of eliminating marginal devices, those with inherent defects or defects resulting from manufacturing aberrations which are evidenced as time and stress dependent failures. In the absence of burn-in, these defective devices would be expected to result in infant mortality or early lifetime failures under use conditions. Therefore, it is the intent of this screen to exercise all elements of the microcircuits at maximum rated operating conditions or to apply equivalent screening conditions which will reveal all time and stress dependent failure modes with equal or greater sensitivity.

2. APPARATUS. The apparatus required for the conduct of this test shall consist of suitable chambers to maintain the devices at specified test temperature and provide access to specified electrical connections, and appropriate electrical test equipment to provide the required electrical inputs and perform the specified intermediate and endpoint measurements.

3. PROCEDURE. The microelectronic device shall be subjected to the burn-in screen at the temperature and for the time specified. The device shall be operated under the specified test condition (see 3.1). Lead, stud or case mounted devices shall be mounted by the leads, stud or case in their normal mounting configuration and the point of connection shall be maintained at a temperature not less than the specified temperature. Intermediate and endpoint measurements shall be made as specified.

3.1 Test conditions. The microelectronic devices shall be subjected to the specified test condition as described below for the specified time and temperature and the required measurements shall be made at the specified intermediate points and endpoints.

(a) Test condition A. Steady state, reverse bias. This test condition is illustrated in figure 1005-1 of method 1005 and is suitable for use on all types of circuits, linear or digital types. In this test as many junctions as possible shall be reverse biased to the specified voltage and power dissipation. The ambient test temperature shall be the maximum possible but shall be selected so as not to exceed the thermal rating of the device.

(b) Test condition B. Steady state, power. This test condition is illustrated in figure 1005-1 of method 1005 and can be used on all digital type circuits and on some linear types. In this test, as many junctions as possible shall be forward biased as specified. The ambient test temperature shall be the maximum possible but shall be selected so as not to exceed the thermal rating of the device.

(c) Test condition C. Steady state, power and reverse bias. This test condition is illustrated in figure 1005-1 of method 1005 and is used strictly on digital type circuits where the inputs can be reverse-biased and the output can be biased for maximum power dissipation or vice versa. The ambient temperature shall be selected so as not to exceed the maximum thermal rating of the device.

(d) Test condition D. Parallel excitation. This test condition is illustrated in figure 1005-2 of method 1005 and is suitable for use on all circuit types. Each circuit is driven with an appropriate signal to simulate as closely as possible circuit application. All circuits shall have a maximum load applied, the excitation shall be applied at a frequency of no less than 60 Hz, and the test shall be conducted at the maximum rated temperature unless otherwise specified. This test is usually referred to as parallel switching applied to digital circuits.

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METHOD 1015 - Continued

(e) Test condition E. Ring oscillator. In this test, illustrated in figure 1005-3 of method 1005, any number of digital circuits greater than two are connected in series. For circuits that cause phase inversion, an odd number of circuits should be used with the output of the last circuit connected to the input of the first circuit. The series will be free running at a frequency established by the propagation delay of each circuit and its associated wiring. Each circuit in the ring shall be loaded to its rated maximum and biased at normal rated voltage. The test shall be conducted at maximum rated temperature unless otherwise specified. This test may be conducted with the open-ring or series switching configuration where the first device in the series is switched by an external source. In this configuration, the duty cycle and the basic frequency of operation depend mainly on the capabilities of the individual devices. When the free running or "closed" ring configuration is employed, no more than 21 devices shall be contained in any single ring. Where the "open" ring configuration is employed, the time duration between inputs from the external source shall be no greater than 20 times the propagation delay of the device as specified in the detail specification. While this test condition affords the opportunity to continuously monitor the test for catastrophic failures (i.e., ring stoppage), this shall not be considered acceptable as a substitute for intermediate measurements, when required.

3.2 Measurements. Endpoint measurements shall be made at 0 hours and at the specified endpoint $^{+72}_{-0}$ hours and, unless otherwise specified, shall consist of all device electrical parameters specified in the applicable procurement document, including parameters specified at temperature extremes. When required by the applicable procurement document, intermediate measurements shall be made at 48 $^{+24}_{-0}$ hours and 96 $^{+24}_{-0}$ hours. These intermediate measurements, unless otherwise specified, shall consist of major functional characteristics of the device under test sufficient to reveal both catastrophic and degradation failures to specified limits, and may be conducted either while the devices are at test temperature, at rated operating temperature limits, or at 25°C upon removal of the devices from the test chamber. When devices are measured at 25°C, they shall be cooled from the test temperature to 25°C prior to removal of bias voltage(s) and all electrical measurements shall be completed within 96 hours from the time bias is removed. When the ring oscillator configuration of test condition E is employed, or in any other configuration where a failure in electrical test equipment, test connections, or test chambers can result in removal of stress on the devices under test which may not be detected prior to the next intermediate test point, the test setup shall be monitored at least once every 24 hours (and preferably once every shift) to establish that the test is still functioning. When a failure is detected, corrective action shall be taken immediately and if the monitoring period exceeds 10 percent of the total burn-in time specified, the affected ring or portion of the inspection lot shall be exposed to an additional period of test equal to the duration of the monitoring period. Where more than one such failure occurs resulting in an accumulation of down-time which exceeds 10 percent of the specified burn-in period the accumulated total time in monitoring periods shall be added to the specified total test time. Where continuous monitoring is employed using strip chart recorders or other means for logging accumulated effective burn-in time or total down-time, the total test duration shall be adjusted to provide the specified minimum hours of actual burn-in time in any case where the down-time exceeds 10 percent of the specified burn-in duration.

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METHOD 1015 - Continued

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test duration. Unless otherwise specified, the minimum test duration shall be 168 hours.
(b) Test condition letter (see 3.1).
(c) Endpoint measurements (see 3.2).
(d) Intermediate measurements (see 3.2), when required.
(e) Criteria for failure for endpoint and intermediate measurements (see 3.2), if other than device specification limits.
(f) Requirements for inputs, outputs, biases, and power dissipation, as applicable (see 3.1).

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METHOD 2001

CONSTANT ACCELERATION

1. PURPOSE. The constant acceleration test is used to determine the effects on microelectronic devices of a centrifugal force. This test is an accelerated test designed to indicate types of structural and mechanical weaknesses not necessarily detected in shock and vibration tests. It may be used as a high stress test to determine the mechanical limits of the package, internal metallization and lead system, die or substrate attachment, and other elements of the microelectronic device. By establishing proper stress levels, it may also be employed as an in-line 100 percent screen to detect and eliminate devices with lower than nominal mechanical strengths in any of the structural elements.

2. APPARATUS. Constant acceleration tests shall be made on an apparatus capable of applying the specified centrifugal force.

3. PROCEDURE. The device shall be restrained by its case, or by normal mountings, and the leads or cables secured. Unless otherwise specified, a centrifugal acceleration of the value specified shall then be applied to the device for 1 minute in each of the orientations X_1, X_2, Y_1, Y_2, Z_1, and Z_2. The applifed centrifugal force shall be as specified (see 4) from the following test conditions:

Test condition	Stress level (G)
A	5,000
B	10,000
C	15,000
D	20,000
E	30,000
F	50,000
G	75,000
H	100,000
J	125,000

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Amount of centrifugal force to be applied, in gravity units (G) (see 3).
  Unless otherwise specified, test condition D shall apply.
(b) Measurements to be made after test.
(c) Any variations in or limitations to orientation (e.g., Y_1 only) (see 3).
(d) Sequence of orientations if other than as specified (see 3).

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METHOD 2002

SHOCK

1. PURPOSE. The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shocks of this type may disturb operating characteristics or cause damage similar to that resulting from excessive vibration, particularly, if the shock pulses are repetitive.

2. APPARATUS. The shock-testing apparatus shall be capable of providing shock pulses of 500 to 30,000 G (peak) as required with a pulse duration between 0.1 and 1.0 msec, to the body of the device.

3. PROCEDURE. The shock-testing apparatus shall be mounted on a sturdy laboratory table or equivalent base and leveled before use. The device shall be rigidly mounted or restrained by its case with suitable protection for the leads. Means may be provided to prevent the shock from being repeated due to "bounce" in the apparatus. Unless otherwise specified, the device shall be subject to 5 shock pulses of the peak (G) level specified in the selected test condition and for a pulse duration of between 0.1 and 1.0 msec in each of the orientations X_1, X_2, Y_1, Y_2, Z_1, and Z_2. Specified measurements shall be conducted after shock and during shock, where applicable.

Test condition	G level (peak)
A	500
B	1,500
C	3,000
D	5,000
E	10,000
F	20,000
G	30,000

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition and duration of pulse (see 3). Unless otherwise specified, test condition B shall apply.
(b) Number and direction of blows if other than specified (see 3).
(c) Electrical-load conditions, if applicable (see 3).
(d) Measurements after shock.
(e) Measurements during shock, if applicable.

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METHOD 2003

SOLDERABILITY

1. PURPOSE. The purpose of this test method is to determine the solderability of all solid and stranded wires up to 1/8 inch thickness, ribbon leads up to 0.050 inches in width and up to 0.025 inches in thickness, and lugs, tabs, hook leads, turrets, etc., which are normally jointed by a soldering operation. This determination is made on the basis of the ability of these terminations to be wetted or coated by solder, or to form a suitable fillet when dip soldered. These procedures will verify that the treatment used in the manufacturing process to facilitate soldering is satisfactory and that it has been applied to the required portion of the part which is designed to accommodate a solder connection. An accelerated aging test is included in this test method which simulates a minimum of 6 months natural aging under a combination of various storage conditions that have different deleterious effects.

2. APPARATUS.

2.1 Solder pot. A solder pot of sufficient size to contain at least two pounds of solder shall be used. This apparatus shall be capable of maintaining the solder at the temperature specified in 3.4.

2.2 Dipping device. A mechanical dipping device capable of controlling the rates of immersion and emersion of the terminations and providing a dwell time (time of total immersion to the required depth) in the solder bath as specified in 3.4 shall be used.

2.3 Optical equipment. An optical system having a magnification of ten diameters shall be used.

2.4 Container and cover. A nonmetallic container of sufficient size to allow the suspension of the specimens 1-1/2 inches above the boiling distilled water shall be used. (A 2,000 ml beaker is one size that has been used satisfactorily for smaller components.) The cover shall be of one or more stainless steel plates and shall be capable of covering approximately 7/8 of the open area of the container so that a more constant temperature may be obtained. A suitable method of suspending the specimens shall be improvised. Perforations or slots in the plates are permitted for this purpose.

2.5 Materials.

2.5.1 Flux. The flux shall conform to type A or W, as applicable, or MIL-F-14256, "Flux, Soldering, Liquid (Rosin Base)."

2.5.2 Solder. The solder shall conform to type S, composition Sn60, of QQ-S-571, "Solder; Tin Alloy; Lead-Tin Alloy; and Lead Alloy."

3. PROCEDURE. The test procedure shall be performed on the number of terminations specified in the applicable procurement document. During handling, care shall be exercised to prevent the surface to be tested from being abraided or contaminated by grease, perspirants, etc. The test procedure shall consist of the following operations:

(a) Proper preparation of the specimens (see 3.1), if applicable.
(b) Aging of all specimens (see 4.2).
(c) Application of flux and immersion of the terminations into molten solder (see 3.3).
(d) Examination and evaluation of the tested portions of the terminations upon completion of the solder-dip process (see 3.5).

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METHOD 2003 - Continued

3.1 Preparation of terminations. No wiping, cleaning, scraping, or abrasive cleaning of the terminations shall be performed. Any special preparation of the terminations, such as bending or reorientation prior to the test, shall be specified in the applicable procurement document. If the insulation on stranded wires must be removed, it shall be done in a manner so as not to loosen the strands in the wire.

3.2 Aging. Prior to the application of the flux and subsequent solder dips, all specimens assigned to this test shall be subjected to aging by exposure of the surfaces to be tested to steam in the container specified in 2.4. The specimens shall be suspended so that no portion of the specimen is less than 1-1/2 inches above the boiling distilled water with the cover specified in 2.4 in place for 60 minutes, minimum. Means of suspension shall be a nonmetallic holder. If necessary, additional hot distilled water may be gradually added in small quantities so that the water will continue to boil and the temperature will remain essentially constant.

3.3 Application of flux. Flux, type W, shall be used (see 2.5.1). Terminations shall be immersed in the flux, which is at room ambient temperature, to the minimum depth necessary to cover the surface to be tested. Unless otherwise specified in the applicable procurement document, terminations shall be immersed to within 0.05 inch of the body of the part. The surface to be tested shall be immersed in the flux for a period of from 5 to 10 seconds.

3.4 Solder dip. The dross and burned flux shall be skimmed from the surface of the molten solder specified in 2.5.2. The molten solder shall be maintained at a uniform temperature of 260° C max (5002F). The surface of the molten solder shall be skimmed again just prior to immersing the terminations in the solder. The part shall be attached to a dipping device (see 2.2) and the flux-covered terminations immersed once in the molten solder to the same depth specified in 3.3. The immersion and emersion rates shall be 1 ± 1/4 inch per second and the dwell time in the solder bath shall be 5 ± 1/2 seconds, unless otherwise specified. After the dipping process, the part shall be allowed to cool in air. Residue flux shall be removed from the terminations by sequential rinses in perchlorethylene and isopropyl alcohol. If necessary, a soft damp cloth moistened with clean 91 percent isopropyl alcohol shall be used to remove all remaining flux.

3.5 Examination of terminations. After each dip-coated termination has been thoroughly cleaned of flux, the 1-inch portion of the dipped lead nearest the component, or the whole lead if less than 1 inch, or the fillet area (whichever is applicable), shall be examined using 10 power magnification (see 2.3).

3.5.1 Evaluation of solid wire terminations 0.045 inch or less in diameter, stranded wire No. 18 AWG or smaller and ribbon leads. The criteria for acceptable solderability during the evaluation of the terminations are:

(a) That the termination is at least 95 percent covered by a continuous new solder coating.
(b) That pinholes or voids are not concentrated in one area and do not exceed 5 percent of the total area.

The area of the surface to be tested as specified in 3.5 shall be examined; if any view of the tested surface shows less than 95 percent coverage, the entire lot shall be rejected. In the case of dispute, the percentage of coverage with pinholes or voids shall be determined by the actual measurement of these areas, as compared to the total area.

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METHOD 2003 - Continued

3.5.2 Evaluation of lugs, tabs, stranded wire greater than No. 18 AWG sizes and solid wire greater than 0.045 inch diameter. The criteria for acceptable solderability during evaluation of the terminations and wires are:

(a) That 95 percent of the total length of fillet, which is between the termination and a connection made to it which typifies the normal connection configuration, be tangent to the surface of the termination being tested and be free from pinholes, voids, etc.
(b) That a ragged or interrupted line at the point of tangency between the fillet and the termination under test shall be considered a defect and included in (a) above.

In case of dispute, the percent of fillet-length with defects shall be determined by actual measurement.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) The number of terminations of each part to be tested (see 3).
(b) Special preparation of the terminations, if applicable (see 3.1).
(c) Depth of immersion if other than 0.05 inch (see 3.3).
(d) Solder dip (see 3.4).
(e) Examination of terminations (see 3.5).
(f) Measurements after test, where applicable.
(g) Solder composition, flux, and temperature if other than those specified.
(h) Number of cycles, if other than one. Where more than one cycle is specified to test the resistance of the device to heat as encountered in multiple solderings, the examinations and measurements required shall be made at the end of the first cycle and again at the end of the total number of cycles applied. Failure of the device on any examination and measurement at either the one-cycle or the end point shall constitute failure to meet this requirement.

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METHOD 2004

LEAD INTEGRITY

1. PURPOSE. This method provides various tests for determining the integrity of microelectronic device leads, welds and seals. Test condition A provides for straight tensile loading. Test condition B_1 provides for application of bending stresses to determine integrity of leads, seals, and lead plating while B_2 employs multiple application of bending stresses primarily to determine the resistance of the leads to metal fatigue under repeated bending. Test conditions C_1 and C_2 provide for application of torque or twisting stresses to device leads or studs, respectively, to determine integrity of leads and seals. It is recommended that this test be followed by a seal test in accordance with method 1014 to determine any effect of the stresses applied on the seal as well as on the leads.

2. APPARATUS. See applicable test condition.

3. PROCEDURE. The device shall be subjected to the stresses described in the specified test condition and in figure 2004-1 and 2004-2, as applicable, and the specified end point measurements shall be made. The force shall be applied to every other lead of each device except that for devices containing more than 10 leads, not more than 5 leads per device need be tested. Where applicable, the leads shall be tested in a cyclical manner; that is, leads numbered 1, 3, etc., on the first device; 2, 4, etc., on the second device; and so on. When a seal test in accordance with method 1014 is conducted as a post test measurement following the lead integrity test(s), meniscus cracks shall not be cause for rejection of devices unless otherwise specified.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition letter.
(b) Number and selection of leads to be tested. Unless otherwise specified, all leads on the device shall be tested in accordance with the specified test condition, excepting test condition B_2 which specifies every other lead.

TEST CONDITION A. TENSION

1. PURPOSE. This test is designed to check the capabilities of the device leads, welds, and seals to withstand a straight pull.

2. APPARATUS. The tension test requires suitable clamps, vise, and hand vice for securing the device and for securing the specified weight to the device lead without lead restriction.

3. PROCEDURE. The specified weight shall be applied, without shock, to each lead or terminal. The case of the device shall be held in a fixed position. When testing axial lead devices, the device shall be supported, with the leads in a vertical position, by securing one lead to a clamp or vise. With a hand vise, or equivalent, the specified weight, including the attaching device, shall be fastened to the lower lead for the time specified. Each lead shall be fastened as close to its end as practicable. When examined using 10X magnification after removal of the stress, any evidence of breakage, loosening, or relative motion between the terminal (lead) and the device body shall be considered a device failure.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Weight to be attached to lead (see 3). Unless otherwise specified, a weight of 12 ounces shall be applied.
(b) Length of time weight is to be attached (see 3). Unless otherwise specified, the weight shall be applied for a minimum of 30 seconds.

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METHOD 2004 - Continued

TEST CONDITION B_1. BENDING STRESS

1. PURPOSE. This test is made to check the quality of the leads, lead welds, and seals of the devices.

2. APPARATUS. Bending-stress tests shall be made using attaching devices, such as suitable clamps or other supports for stud-mounted devices.

3. PROCEDURE. The specific procedure of 3.1, 3.2, or 3.3 shall be followed, as applicable, to the specific device type under test.

3.1 Procedure for cylindrical devices. With the lead of the device held in a suitable clamp, the specified force shall be applied, without shock, at right angles to the reference axis of the device, as near the top of the opposite contact or tubulation as practicable. The force shall be applied once in each of two mutually perpendicular directions, both directions being perpendicular to the original lead position. The lead shall be returned to normal following each application. For a device lead which bends noticeably when less than the specified force is applied, the bend shall be continued until the specified force is achieved or until the bend equals 90^{+10}_{-0} degrees, whichever condition occurs first.

3.2 Procedure for stud-mounted devices. The device shall be securely fastened, with its reference axis in a horizontal position, by screwing the stud into a suitable support. With a hand vise, or equivalent, the specified weight shall be suspended from the hole in the lug for the length of time specified.

3.3 Procedure for ribbon or tab lead devices. For devices with ribbon or tab leads, a force of 8.0 ± 1.0 ounce, unless otherwise specified, shall be applied to the lead at a distance of 0.12 ± 0.03 inch from the device body or at the end of the lead if it is shorter than 0.12 inch. The force shall be applied to each lead once in each of two mutually perpendicular directions, both directions being perpendicular to the original lead position. When devices have leads which are formed close to the body, the forces may be applied 0.12 ± 0.03 inch from the form. Bending forces shall be applied in accordance with the applicable diagram of figure 2004-1 of this test method. For a device lead which bends noticeably when less than the specified force is applied, the bend shall be continued until the specified force is achieved or until the bend equals 90^{+10}_{-0} degrees, whichever condition occurs first. The lead shall then be restored to its original position. For ribbon lead flat packs (such as the TO-84 and TO-89 packages) where the lead cross section is 0.002 x 0.020 inches or less and the width to thickness ratio is greater than 8 to 1, a force of 3 ± 0.3 ounces shall be applied instead of the 8 ounce force specified above and the lead bend shall not be applied to the end leads of packages (such as the TO-89 package) where the application of the bending stress will apply primarily torsion at the lead seal.

3.4 Measurements. When examined using magnification between 10X and 20X after removal of the stress, any evidence of breakage, loosening, or relative motion between the terminal lead and the device body shall be considered a device failure. Specified post-test measurements (see 4) shall be made after visual examination.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Special preparations or conditions, if required.
(b) Weight to be attached to lead (see 3.1 and 3.2, and 3.3, if other than the specified weight).
(c) Specific procedure (see 3.1, 3.2, and 3.3).
(d) Length of time weight is applied, where applicable (see 3.1 and 3.2).
(e) Measurements to be made after test (see 3.4).

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METHOD 2004 - Continued

TEST CONDITION B_2. LEAD FATIGUE

1. PURPOSE. This test is to check the resistance of the device leads to metal fatigue.

2. APPARATUS. The lead fatigue test shall be made using the specified weight and with suitable clamping or attaching devices.

3. PROCEDURE. A force of 8.0 ± 1.0 ounce, unless otherwise specified, shall be applied to the lead at a distance of 0.12 ± 0.03 inch. When devices have leads which are formed close to the body, the forces may be applied 0.12 ± 0.03 inch from the device body or at the end of the lead if it is shorter than 0.12 inch. The forces shall be applied in the force #1 direction as described in figure 2004-1 of this test method for a minimum of three complete bending cycles through a $90 {}^{+10}_{-0}$ degree arc of the case with return to normal. For a device lead which bends noticeably when less than the specified force is applied, the bend shall be continued until the specified force is achieved or until the bend equals $90 {}^{+10}_{-0}$ degrees, whichever condition occurs first. The lead shall then be restored to normal position. For ribbon lead flat packs (such as the TO-84 and TO-89 packages) where the lead cross section is 0.002 x 0.020 inches or less and the width to thickness ratio is greater than 8 to 1, a force of 3 ± 0.3 ounces shall be applied instead of the 8 ounce force specified above and the lead bend conditioning shall not be applied to the end leads of packages (such as the TO-89 package) where the application of the bending stress will apply primarily torsion at the lead seal. Any evidence of breakage, loosening or relative motion between the terminal (board) and the device body or damage to lead plating, when examined at a magnification between 10X and 20X after removal of the stress, shall be considered a device failure. Specified post-test measurements (see 4) shall be made after visual examination.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Force to be applied to the lead, if other than the specified weight (see 3).
(b) Number of bending cycles, if more than three (see 3).
(c) Measurements to be made after this test.
(d) Maximum bend angle, if other than 90 degrees (see 3).
(e) Direction of force application if other than force #1 direction (see 3).

TEST CONDITION C_1. LEAD TORQUE

1. PURPOSE. This test is designed to check device leads (or terminals) and seals for their resistance to twisting motions.

2. APPARATUS. The torque test requires suitable clamps and fixtures, and a torsion wrench or other suitable method of applying the specified torque without lead restriction.

3. PROCEDURE. The body of the device shall be securely clamped, with a suitable fixture, and the specified torque shall be applied to the portion of the lead to each lead of the device, without shock, about the axis of the lead. The torque shall be applied between the lead and the case, in a direction which tends to cause loosening of the lead.

3.1 Ribbon pin or tab lead devices. For devices with ribbon pin or tab leads, a torque of 2.0 ± 0.2 ounce-inch, unless otherwise specified, shall be applied to the lead at a distance of 0.12 ± 0.03 inch from the device body or at the end of the lead if it is shorter than 0.12 inch. The torque shall be applied about the axis of the lead once in each direction (clockwise and counterclockwise). When devices have leads which are formed close to the body, the torque may be applied 0.12 ± 0.03 inch from the form. For device leads which twist noticeably when less than the specified torque is applied,

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METHOD 2004 - Continued

the twist shall be continued until the specified torque is achieved or until the twist equals 30 ± 10 degrees, whichever condition occurs first. The lead shall then be restored to its original position. Torque shall be applied in accordance with the applicable diagram of figure 2004-2 of this test method.

3.2 Measurements. When examined using magnification between 10X and 20X after removal of stress, any evidence of breakage, loosening, or relative motion between the terminal lead and the device body shall be considered a device failure. Specified post-test measurements (see 4) shall be made after visual examination.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Measurements to be made after test (see 3.2).
(b) Number of twist cycles if more than 1 (see 3 and 3.1).
(c) The magnitude of torque to be applied, if other than 2.0 ounce-inch (see 3).
(d) The angle of twist, if other than 30° (see 3).

TEST CONDITION C_2. STUD TORQUE

1. PURPOSE. This test is designed to check the resistance of the device with threaded mounting stud to the stress caused by tightening the device when mounting.

2. APPARATUS. The torque test requires suitable clamps and fixtures, and a torsion wrench or suitable method of applying the specified torque.

3. PROCEDURE. The device shall be clamped by its body or flange. A flat steel washer of minimum thickness equal to six thread pitches and a new class 2 fit steel nut shall be assembled in that order on the stud, with all parts clean and dry. The specified torque shall be applied without shock to the nut. The nut and washer shall then be disassembled from the device, and the device then examined for compliance with the requirements. The device shall be considered a failure if:

(a) The stud breaks or is elongated greater than 1/2 of the thread pitch.
(b) It fails the specified post-test end point measurements.
(c) There is evidence of thread stripping or deformation of the mounting seat.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) The amount of torque to be applied (see 3).
(b) Length of time torque is to be applied (see 3).
(c) Measurements to be made after test (see 3).

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METHOD 2004 - Continued

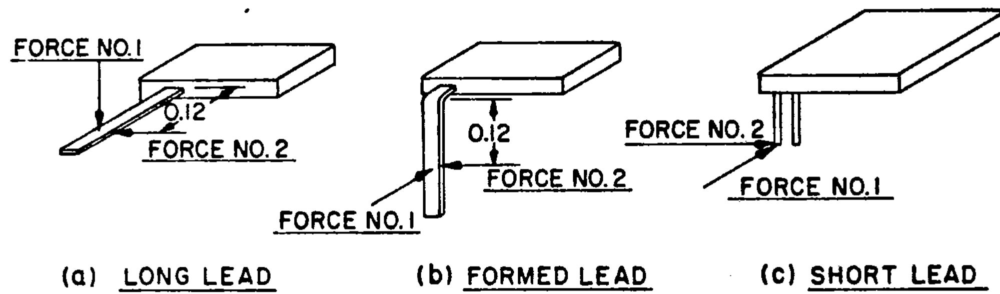

FIGURE 2004-1. Bending stress force application.

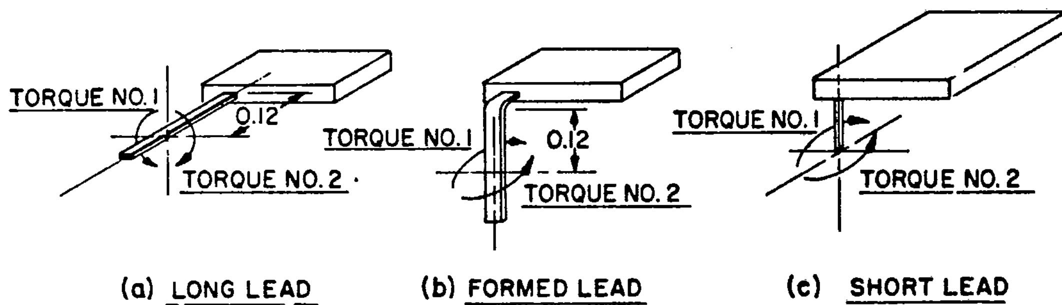

FIGURE 2004-2. Torsion stress torque application.

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METHOD 2005

VIBRATION FATIGUE

1. PURPOSE. The purpose of this test is to determine the effect on the device of vibration in the frequency range specified.

2. APPARATUS. Apparatus for this test shall include equipment capable of providing the sustained vibration within the specified levels and the necessary optical and electrical equipment to conduct post-test measurements.

3. PROCEDURE. The device shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. Lead-mounted devices shall be mounted by their leads in the normal mounting configuration. The device shall be vibrated with a constant amplitude simple harmonic motion having a peak acceleration corresponding to the specified test condition. For test condition A, constant amplitude harmonic motion in the range of 60 ± 20 Hz having an amplitude of 0.06 inches double amplitude (total excursion) shall be acceptable as an alternative to the specified peak acceleration. The vibration shall be applied for 32 ± 8 hours minimum, in each of the orientations X, Y, and Z for a total of 96 hours, minimum. Following vibration, the device shall be subjected to the specified post-test measurements and to an external visual examination at a magnification between 10X and 20X for evidence of damage to package, leads, seals, and markings. When specified, devices with an internal cavity containing parts or elements subject to possible movement or breakage during vibration shall be further examined by radiographic examination in accordance with test method 2012 or by delidding or opening and internal visual examination at 30X magnification to reveal damage or dislocation. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

Test condition	Peak acceleration, G
A - - - - - - - - - -	20
B - - - - - - - - - -	50
C - - - - - - - - - -	70

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition (see 3).
(b) Test frequency (see 3), if other than specified.
(c) Test time and specimen orientation, if other than specified (see 3).
(d) Measurements after test (see 3).

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METHOD 2006

VIBRATION NOISE

1. PURPOSE. The purpose of this test is to measure the amount of electrical noise produced by the device under vibration.

2. APPARATUS. Apparatus for this test shall include equipment capable of providing the required variable frequency vibration at the specified levels, a calibrated high impedance voltmeter for noise measurement during test and the necessary optical and electronic equipment for post-test measurements.

3. PROCEDURE. The device and its leads shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. Lead-mounted devices shall be mounted by their leads in the normal mounting configuration. The device shall be vibrated with simple harmonic motion having either an amplitude of 0.06 inch double amplitude (maximum total excursion) or a constant peak acceleration of 20G minimum. The vibration frequency shall be varied approximately logarithmically between 20 and 2,000 Hz. The entire frequency range shall be traversed in not less than 4 minutes for each cycle. This cycle shall be performed once in each of the orientations X, Y, and Z (total of 3 times), so that the motion shall be applied for a total period of approximately 12 minutes. The specified voltages and currents shall be applied in the test circuit. The maximum noise-output voltage across the specified load resistance during traverse, shall be measured with an average-responding root-mean-square (r.m.s.) calibrated high impedance voltmeter. The meter shall measure, with an error of not more than 3 percent, the rms value of a sine-wave voltage at 2,000 hertz (Hz). The characteristic of the meter over a bandwidth of 20 to 2,000 Hz shall be ±1 decibel (db) of the value at 2,000 Hz, with an attenuation rate below 20 and above 20,000 Hz of 6 ± 2 db per octave. The maximum inherent noise in the circuit shall be at least 10 db below the specified noise-output voltage. Following vibration, the device shall be subjected to the specified post-test measurements and to an external visual examination at a magnification between 10X and 20X for evidence of damage to package, leads, seals, and markings. When specified devices with an internal cavity containing parts or elements subject to possible movement or breakage during vibration shall be further examined by radiographic examination in accordance with test method 2012 or by delidding or opening and internal visual examination at 30X magnification to reveal damage of discoloration. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition (see 3).
(b) Test voltages and currents (see 3). Unless otherwise specified, these shall be the nominal operating voltages and currents for the device.
(c) Load resistance (see 3). Unless otherwise specified, this shall be the maximum rated operating load of the device.
(d) Post-test measurement (see 3).
(e) Noise-output voltage limit (see 3).

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METHOD 2007

VIBRATION, VARIABLE FREQUENCY

1. PURPOSE. The variable frequency vibration test is performed for the purpose of determining the effect on component parts of vibration in the specified frequency range. This is a destructive test.

2. APPARATUS. Apparatus for this test shall include equipment capable of providing the required variable frequency vibration at the specified levels and the necessary optical and electrical equipment for post-test measurements.

3. PROCEDURE. The device shall be rigidly fastened on the vibration platform and the leads or cables adequately secured. Lead-mounted devices shall be mounted by their leads in the normal mounting configuration. The device shall be vibrated with simple harmonic motion having an amplitude of either 0.06 inches double amplitude (maximum total excursion) or the peak acceleration for test condition A, B, or C, as specified, whichever is less. The vibration frequency shall be varied approximately logarithmically between 20 and 2,000 Hz. The entire frequency range of 20 to 2,000 Hz and return to Hz shall be traversed in not less than 4 minutes. This cycle shall be performed 4 times in each of the orientations X, Y, and Z (total of 12 times), so that the motion shall be applied for a total period of approximately 48 minutes, minimum. Following vibration, the device shall be subjected to the specified post-test measurements and to an external visual examination at a magnification between 10X and 20X for evidence of damage to package, leads, seals, and markings. When specified, devices with an internal cavity containing parts or elements subject to possible movement or breakage during vibration shall be further examined by radiographic examination in accordance with method 2012 or by delidding or opening and internal visual examination at 30X magnification to reveal damage or dislocation. Where this test is performed as part of a group or subgroup of tests, the post-test measurements or inspections need not be performed specifically at the conclusion of this test, but may be performed once at the conclusion of the group or subgroup.

Test condition	Peak acceleration, G
A	20
B	50
C	70

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition (see 3).
(b) Measurements after test (see 3).

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METHOD 2008

VISUAL AND MECHANICAL

1. PURPOSE. The purpose of this examination is to check the physical dimensions of the device and to verify that materials, design, construction, marking, and workmanship are in accordance with the applicable requirements. This test would normally be employed in initial qualification or periodic requalification of a specific device type to demonstrate compliance with specifications for the specific part or drawing number or to reveal any undocumented changes to the part type.

2. APPARATUS. Equipment used in this examination shall be capable of demonstrating conformance to the requirements of the applicable procurement document which shall include optical equipment capable of magnification between 10X and 20X to reveal structural features of microelectronics devices.

3. PROCEDURE. The device shall be examined in accordance with the requirements of the specified test condition and at a magnification between 10X and 20X.

3.1 Test condition A.

Physical dimensions. The device shall be examined to verify that the physical dimensions are as specified in the applicable procurement document. The specified dimensions shall include, as a minimum, all outline dimensions of the device, the length, width and thickness (or diameter for round or wire leads) of leads, lead spacing, special lead shapes (e.g., required bend positions, angles of bead radii) where applicable, dimensions of any projecting or indented features used for coding of lead arrangement, automatic handling and similar purpose, dimensions, location and symbology of markings or lettering and any other information which affects the installed size or orientation of the device in normal applications.

3.2 Test condition B.

Materials, design, construction, marking, and workmanship. The device shall be examined to verify that the materials, design, construction, marking (including legibility) and workmanship are in accordance with all the applicable requirements of the applicable procurement document, including all internal and external features. Internal features shall be examined by delidding or opening those devices with an internal cavity following the completion of all manufacturing operations. Devices without an internal cavity (e.g., encapsulated or embedded devices) or those which would experience destruction of internal features as a result of opening, may be tested by examination of internal elements in specimens intercepted at various stages in completion of the manufacturing process, as appropriate to the device type.

In addition to the above requirements, in any case where the internal elements of the device are packaged or encapsulated by other than the manufacturer of those internal elements, the internal examination of the microelectronic device shall include the determination that a chip, substrate or other internal element of each device bears a legible trademark or other symbol identifying the manufacturer of the internal elements of the device. The external examination shall also include the determination that the exterior of the package bears a legible trademark or other symbol identifying the manufacturer who packaged the microelectronic device, a lot code or date code traceable to the manufactured lot and approximate time period of manufacture. The absence of these markings shall constitute a device failure.

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METHOD 2008 - Continued

3.2.1 Marking. Unless otherwise specified, two sealed specimens from the group shall be immersed in solvent type A and two specimens in solvent type B, both at a tempeature of 25 ± 2°C, for a period of 10 ± 1 minute. Brush the immersed parts a minimum of five strokes with a short bristle brush in the area of the markings. Remove the parts from the solvents, rinse, and allow to dry. When dry, the markings shall be legible under 4X magnification.

Solvents:

Type A - 100 percent trichloroethylene
Type B - Refrigerant-alcohol mixture (65 percent by weight Freon-113 and 35 percent ethyl alcohol formula 30).

3.2.2 Die topography and interconnection pattern. When required by the applicable procurement document, the topography of elements formed on the die or substrate and the metallization pattern shall be photographed at a magnification of 80X minimum or at sufficient magnification to enlarge the largest die or substrate dimension to a minimum of 8 inches in length, whichever is less. For purposes of comparing the device being tested to determine conformance to a specified topography or interconnection pattern, a photograph of the specified die topography and interconnection pattern shall be provided, at the same magnification as specified in this requirement and any differences between the two photographs shall be recorded.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition (see 3).
(b) Dimensions which are capable of physically describing the device (see 3.1).
(c) Detailed requirements for materials, design, construction, marking, and workmanship (see 3.2).
(d) Requirement for photographic record, if applicable (see 3.2.2), and disposition of photographs.

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METHOD 2009

EXTERNAL VISUAL

1. PURPOSE. The purpose of this examination is to verify that the physical dimensions, materials, design, construction, markings, and workmanship of the device are in accordance with the applicable procurement document. This test would normally be employed on a lot sampling or 100 percent basis at outgoing inspection from the device manufacturers facility, as an incoming user inspection, or as an examination for evidence of physical damage subsequent to application of environmental or mechanical test methods.

2. APPARATUS. Apparatus used in this test shall be capable of demonstrating device conformance to the applicable requirements, which may include optical equipment capable of magnification between 3X and 20X and a relatively large and accessible field of view such as an illuminated ring magnifier.

3. PROCEDURE. The device shall be examined in accordance with the requirements of the applicable procurement document. This examination shall be sufficient to determine that the device dimensions, configuration, lead structure, markings (content, placement and legibility), materials, construction, and workmanship are in accordance with the applicable specification. The device shall be inspected for defects or damage resulting from manufacturing, handling or testing, for visible evidence of corrosion, contamination or breakage (grossly bent or broken leads, cracked seals), defective (peeling, flaking or blistered) or damaged plating and any other features which could interfere with the normal application of the device. These inspections, unless otherwise specified, shall be conducted at a magnification between 3X and 20X. Evidence of any nonconformance with the detail drawings or applicable procurement document, the absence of any required feature, or evidence of damage, corrosion or contamination which could interfere with the normal application of the device shall constitute a failure.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Dimensions and markings capable of physically describing the device, its source of manufacture, its intended function, and the lead or pin arrangement (see 3).
(b) Detailed requirements for materials, design, construction, and workmanship (see 3).
(c) Where applicable, test methods which precede the external visual examination.

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METHOD 2010

INTERNAL VISUAL (PRECAP)

1. PURPOSE. The purpose of this test is to check the internal physical dimensions, materials, design construction, markings, and workmanship of monolithic, multi-chip, film and hybrid microcircuits for compliance with the requirements of the applicable procurement document. This test will be normally be used prior to capping or encapsulation on a 100 percent inspection basis to detect and eliminate devices with internal defects which could lead to device failures in normal application. It may also be employed on a sampling basis to determine the effectiveness of the manufacturers quality control and handling procedures for microelectronic devices.

Test condition A provides rigorous and detailed procedure for internal visual inspection intended for high reliability monolithic and multichip microcircuits. Test condition B provides a procedure with inspection criteria reduced to the minimum considered acceptable for military grade devices. Test condition C provides a rigorous and detailed procedure for internal visual inspection intended for high reliability hybrid microcircuits.

2. APPARATUS. The apparatus for this test shall include optical equipment capable of the specified magnifications (see 3) and any visual standards (gages, drawings, photographs, etc.) necessary to perform an effective examination and enable the operator to make objective decisions as to the acceptability of the device being examined.

3. PROCEDURE. The device shall be examined in a suitable sequence of observations and at the specified magnification to determine compliance with the requirements of the applicable procurement document and the criteria of the specified test condition.

3.1 Test condition A. Procedure for monolithic and multi-chip microcircuits. Internal visual examination prior to capping or encapsulation shall be conducted on all monolithic and multi-chip microcircuits and all similar devices which are employed in hybrid microcircuit types. The order of examination required in paragraphs 3.1.1 through 3.1.14.1 may be varied at the discretion of the manufacturer. All examinations shall be conducted at the specified magnification. All references herein to silicon oxide or oxide shall also apply to any other passivation material used in fabricating monolithic and multi-chip microcircuits.

3.1.1 Metallization defects. Metallization defects are defined as scratches, voids, corrosion or bridged metallization in the interconnecting metallization patterns of monolithic microcircuits. The rejection criteria for microcircuits with metallization defects are:

3.1.2 Metallization scratches and voids. Microscopic examination for metallization scratches and voids will be performed at a minimum magnification of 80X and will be conducted with a binocular microscope with the device under vertical illumination. No device will be acceptable which exhibits:

(a) A scratch or void in the interconnecting metallization which reduces the width of the conducting strip to less than one-half of the minimum designed width, provided the scratch exposes silicon oxide at any point along its length. (See figure 2010-1.)
(b) Any scratch or void in the interconnecting metallization over a contact cut or window if the defect isolates more than 1/2 of the designed contact from the interconnecting metallization. (See figure 2010-1.)
(c) A scratch or void in the bonding pad metallization, exposing silicon oxide, if the scratch isolates more than one-half (1/2) of the bond from the metallization stripe or a scratch in the bonding pad area which reduces the width of the metallization, in front of the bond toward the active region of the circuit, to less than one-half (1/2) of the narrowest design width of the interconnecting metallization connected to the pad. (See figure 2010-1.)
(d) Any scratch or void at, or over, an oxide step which reduces the width of the conducting stripe to less than three-quarters of the minimum designed width. (See detail A of figure 2010-1.)

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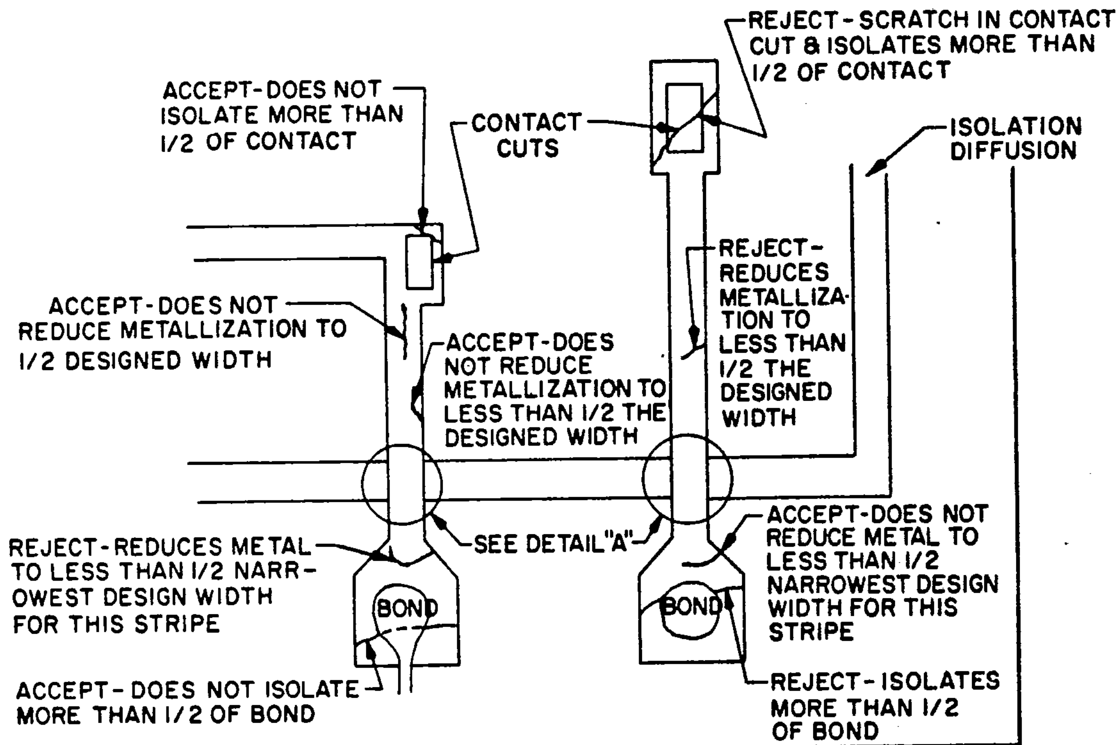
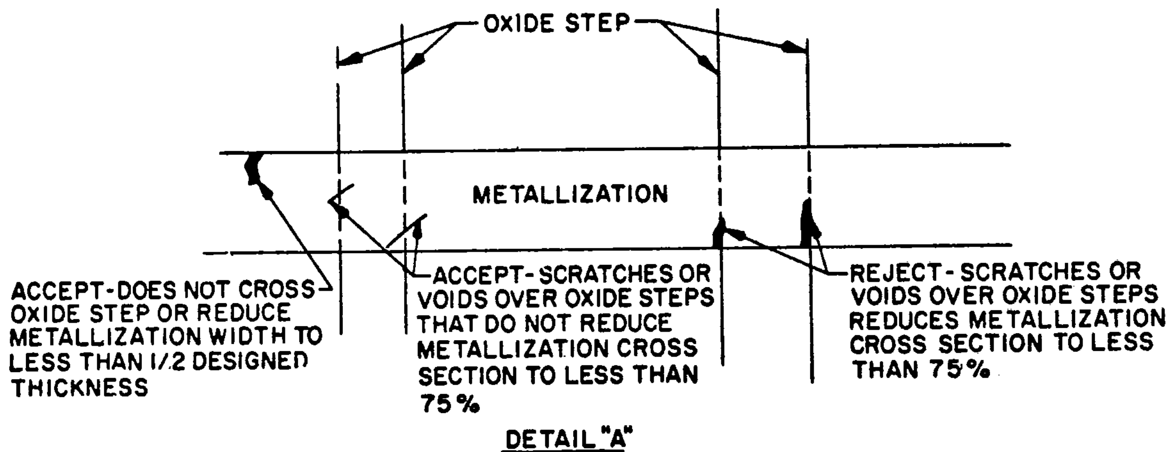
METHOD 2010 - Continued





DETAIL "A"

FIGURE 2010-1

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METHOD 2010 - Continued

3.1.3 Corrosion. Microscopic examination for corrosion will be conducted at a minimum magnification of 80X and will be performed with a binocular microscope with the device illuminated with vertical light.

3.1.3.1 Corrosion defects. Any device with any evidence of corrosion, or lifting or peeling of the interconnecting metallization will be rejected.

3.1.4 Bridged metallization. Microscopic examination for bridged metallization will be conducted at a minimum magnification of 80X with a binocular microscope and the device illuminated with vertical light.

3,1.4.1 Bridged metallization defects. Any device which exhibits bridged metallization defects to the extent that the distance between any two metallization stripes has been reduced to one quarter (1/4) of the designed separation shall be rejected. This bridging may be caused by smears or photolithographic defects (see figure 2010-2).

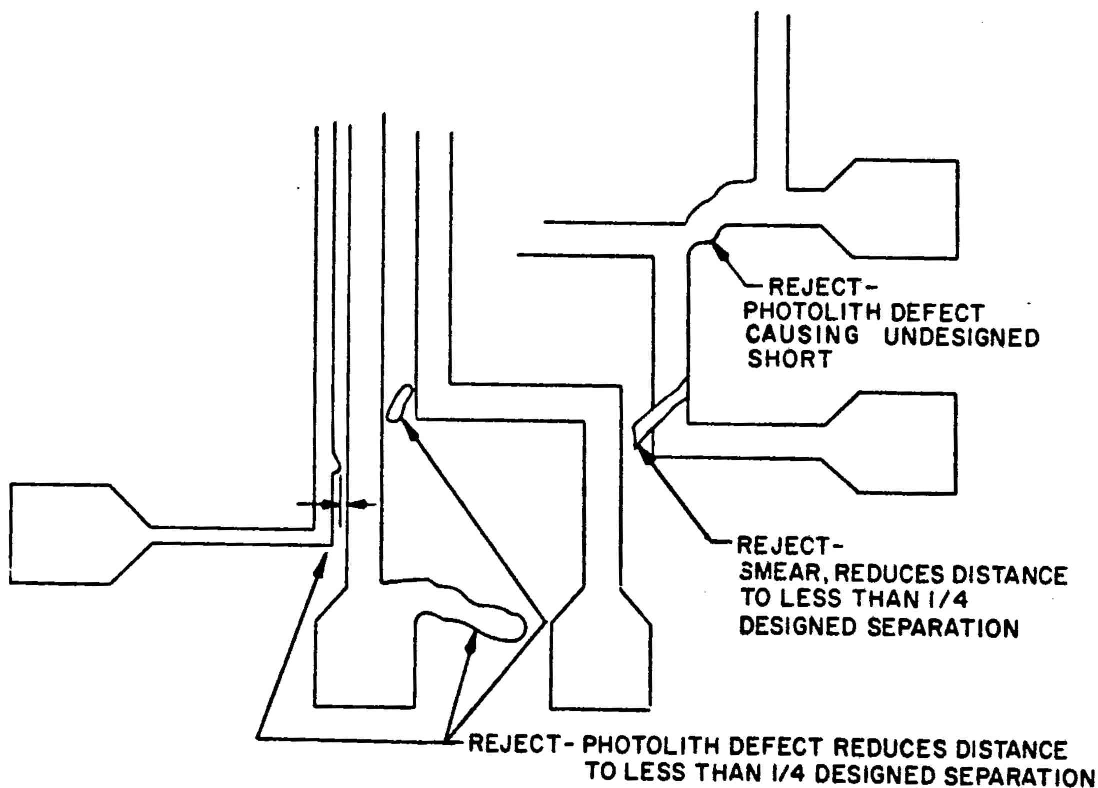

FIGURE 2010-2

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METHOD 2010 - Continued

3.1.5 Metallization alignment. Microscopic examination of the metallization alignment will be made at a minimum magnification of 80X with a binocular microscope and the device illuminated with vertical light.

3.1.5.1 Metallization defects. Any device in which the metallization does not completely cover 1 2 of the designed contact window shall be rejected.

3.1.5.2 Metallization path. Any device in which a metallization path not intended to cover a contact window comes closer than 1/4 of the designed distance to the edge of the contact window shall be rejected.

3.1.6 Exposed junctions. Microscopic examinations of each device for exposed junctions will be conducted at a minimum magnification of 80X utilizing a binocular microscope and with the device illuminated with vertical light.

3.1.6.1 Junction defects. Any device which exhibits any junction area not covered with thermally grown oxide shall be rejected.

3.1.6.2 Contact cut. A contact cut in a diffused area must not extend across a junction into an undiffused area.

3.1.7 Scribed chip inspection. Microscopic inspection of each scribed chip will be conducted at a minimum magnification of 80X with a binocular microscope and the device illuminated with vertical light.

(a) Any scribed chip that does not show 0.5 mils of silicon dioxide between the interconnecting metallization pattern and the edge of the chip shall be rejected (see figure 2010-3).

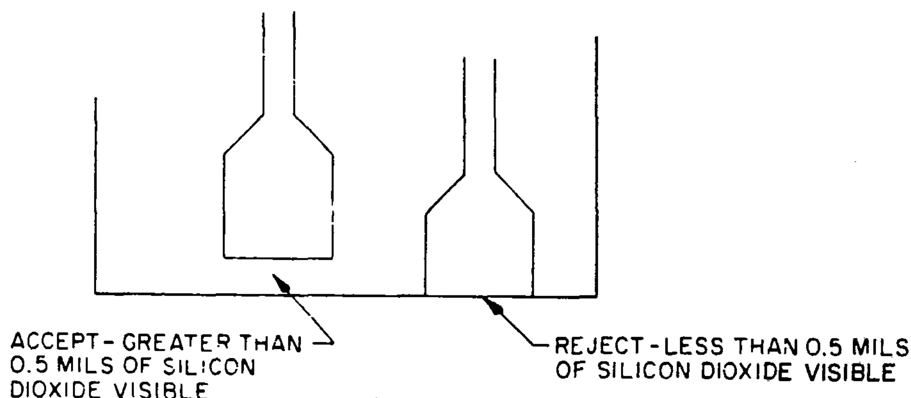

FIGURE 2010-3

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METHOD 2010 - Continued

(b) Chip-outs. Any device which does not have 0.5 mils of silicon dioxide visible between the metallization and/or ball bond periphery and the edge of the chip shall be rejected. Any device with chips out of the oxide in the active circuit areas shall be rejected (see figure 2010-4).

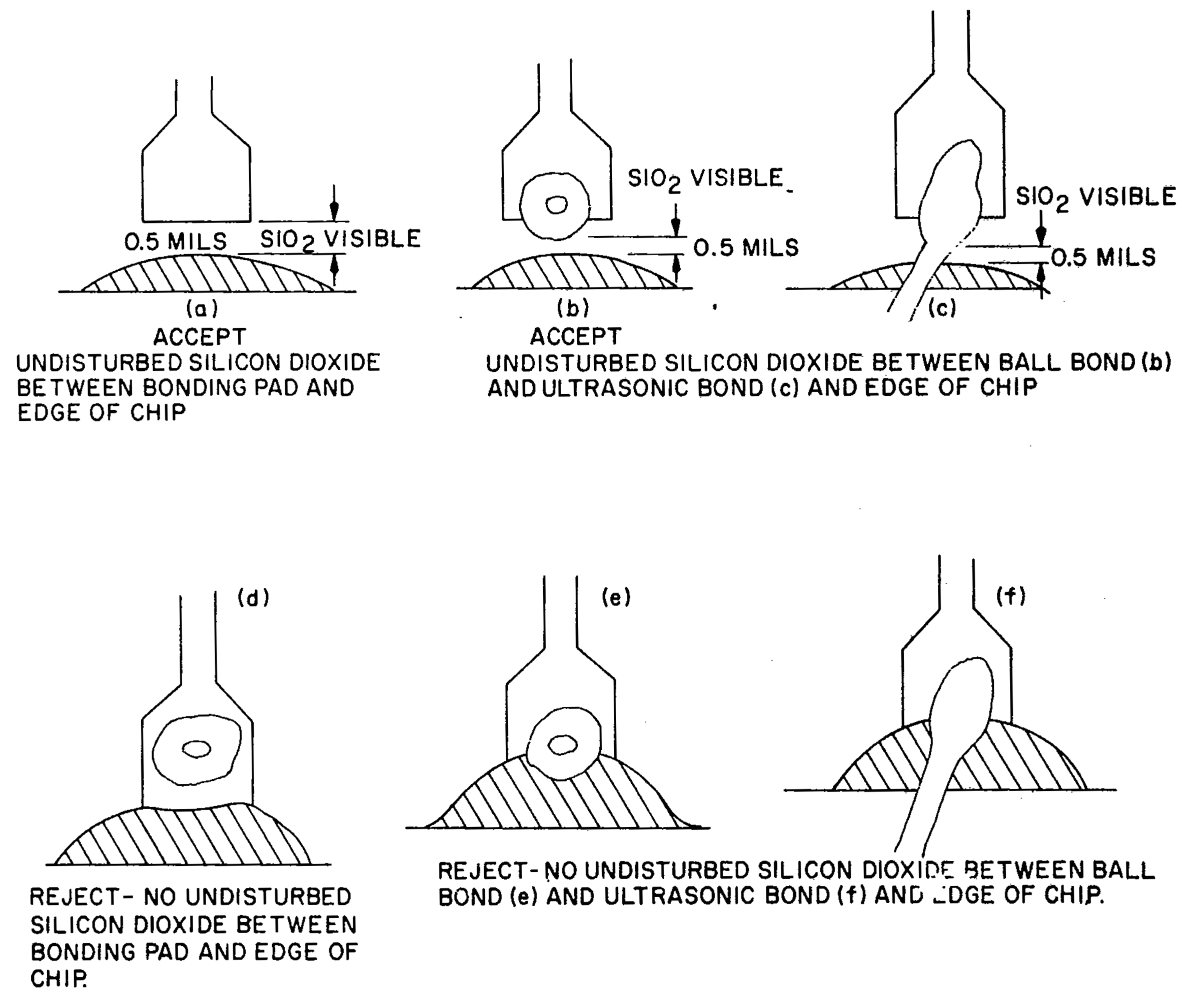

FIGURE 2010-4

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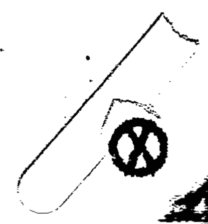

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METHOD 2010 - Continued

(c) Cracks. Any device with a crack in the silicon die that exceeds 1 mil in length and points toward an active area, metallization or bond shall be rejected. Any device with cracks in the active circuit area or in the metallization pad area will be rejected (see figure 2010-5).

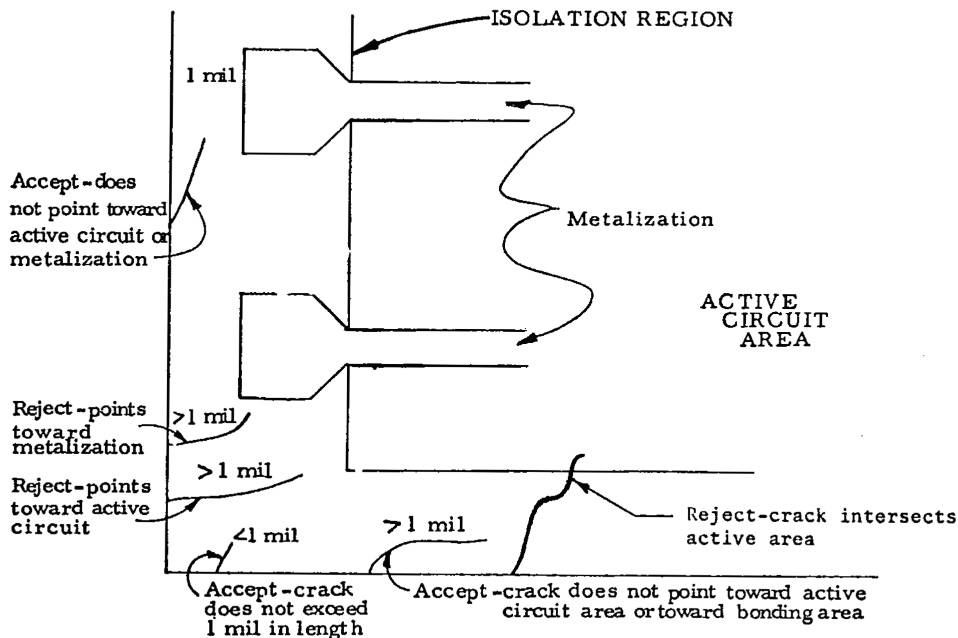

FIGURE 2010-5

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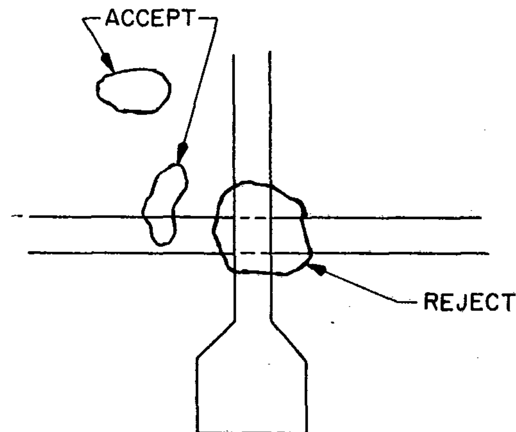
METHOD 2010 - Continued

3.1.8 Oxide defects and diffusion faults. Microscopic inspection of oxide defects and diffusion faults shall be performed at a minimum magnification of 80X with a binocular microscope and with the device illuminated with vertical light.

3.1.8.1 Oxide and diffusion faults. Reject any device in which an oxide defect or diffusion fault:

(a) Connects metallization to a diffused area not already connected by a contact cut to that stripe. (See figure 2010-6.)
(b) Appears to short any two diffused areas. (See figure 2010-7b.)
(c) Causes any diffusion area to be discontinuous. (See figure 2010-7c.)
(d) Exceeds 75 square mils (approximately two bonding pad areas).
(e) Exceeds 15 mils in the longest dimension.
(f) Connects two metallization stripes. (See figure 2010-7a.)
(g) Appears to consist of an absence of oxide under metallization such as to cause a short between the metal and the underlying silicon. Double or triple lines on the edges of the defect indicate that it has depth and may penetrate down to bare silicon. (See figure 2010-7d.)



OXIDE OR DIFFUSION EFFECTS

FIGURE 2010-6

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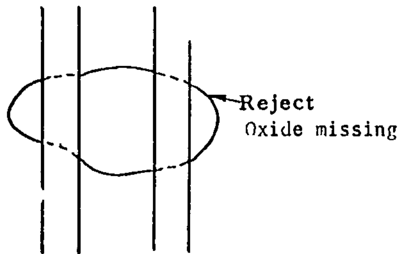
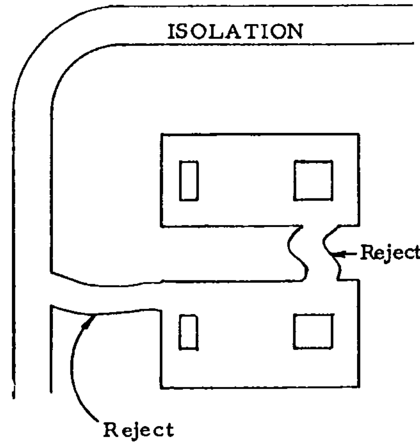
METHOD 2010 - Continued



Oxide faults on or between
METALIZATION STRIPES

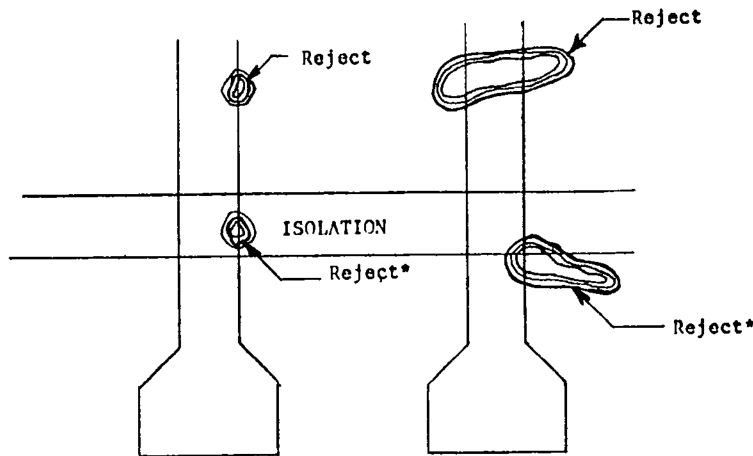
FIGURE 2010-7a



Oxide or diffusion faults

FIGURE 2010-7b

FIGURE 2010-7c



*NOTE: If center of defect is taupe (Brownish-gray) where it lies in a diffused area, there may be no silicon dioxide at this place.

Oxide faults under metallization

FIGURE 2010-7d

Supersedes page 8 of 1 May 1968.

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METHOD 2010 - Continued

3.1.9 Foreign material. Microscopic examination for foreign material will be performed at a minimum magnification of 30X and a maximum magnification of 50X with a binocular microscope and the device illuminated with vertical lighting. Unattached foreign material shall not be acceptable on the surface of the device chip or substrate or within the package. Attached conductive foreign material visible on the chip or substrate surface that bridges any two metallization areas, any two circuit elements or semiconductor junctions or any combination of metallization and circuit element or junction shall not be acceptable. Material shall be considered attached when it can not be removed by a nominal gas blow. Conductive foreign material is defined as any opaque substance.

3.1.10 Bond inspection. Microscopic inspection of bonds will be performed at a minimum magnification of 30X and a maximum magnification of 50X with a binocular microscope and the device illuminated with vertical lighting. Reference to wedge bonds shall apply to ultrasonic bonds, wedge bonds, and other configurations, excluding ball bonds.

3.1.10.1 Bond size.

(a) Ball bond size. Any device with ball bonds to the silicon chips that are less than two times or greater than six times the bonding wire diameter shall be rejected. Any device that exhibits evidence of rebonding on the same pad shall be rejected. Any device where the center of the bonding wire is closer to the ball bond edge than a distance equal to 1/2 the wire diameter shall be rejected.

(b) Ultrasonic bond size. Ultrasonic bonds to the silicon chip that are less than 1.2 times and more than 3.0 times the wire diameter shall be rejected. Any device that exhibits evidence of rebonding shall be rejected.

3.1.10.2 Bond placement.

(a) Ball bonds. Devices containing bonds where less than 50% of the bond is within the pad area shall be rejected. Devices with bonds in the fillet area of the bonding pad that reduce the major distance between the bond periphery and the edge of the fillet to less than 1/2 the narrowest designed width of the interconnecting metallization shall be rejected. (See figure 2010-8.)

(b) Ultrasonic bonds. Devices containing bonds where less than 50% of the bond is within the bonding pad area shall be rejected. Devices with bond tails longer than 3 mils in length shall be rejected. Devices with bonds in the fillet area of the bonding pad that reduce the major distance between the bond area and the fillet to less than 1/2 the narrowest designed width of the interconnecting metallization shall be rejected. (See figure 2010-8.)

(c) General. Devices with bonds placed so that the wire from the bond passes over another metal bonding pad shall be rejected. Devices with bonds places so that the separation between the bonds or the bond and adjacent metallization is less than 0.5 mil shall be rejected. (See figure 2010-9.)

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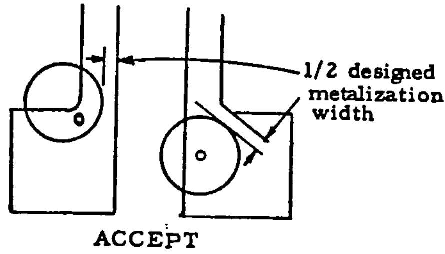
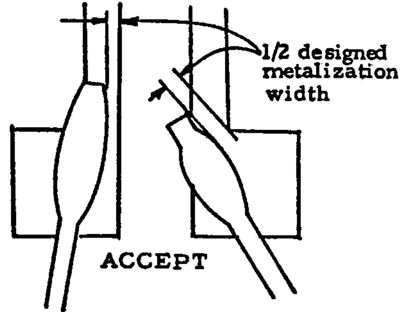
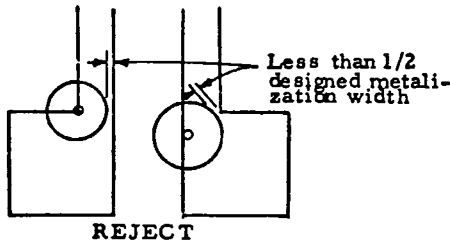
METHOD 2010 - Continued

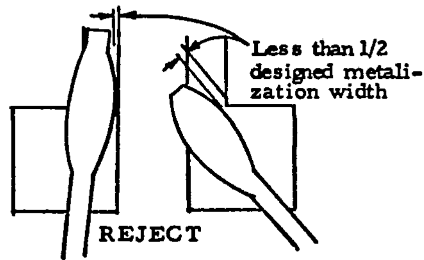
BALL BONDS

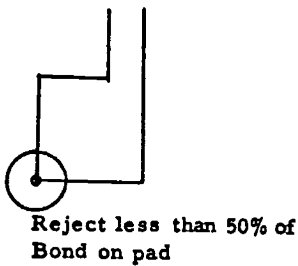
ULTRASONIC BONDS

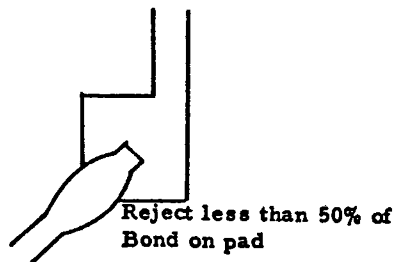


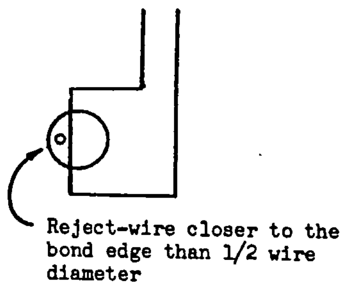












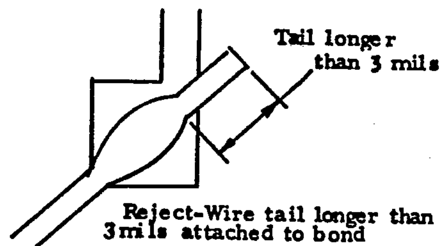


FIGURE 2010-8

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METHOD 2010 - Continued

Periphery of unoxidized Silicon

Reject - Bond over unoxidized silicon

Reject - Bond over unoxidized silicon

Less than 0.5 mils

Reject - Bonds in too close proximity

Less than 0.5 mils

Reject - Bonds in too close proximity

Less than 0.5 mils

Reject - Bond in too close proximity with adjacent bonding pad

Less than 0.5 mils

Reject - Bonds in too close proximity

FIGURE 2010-9

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METHOD 2010 - Continued

3.1.11 Bonding at package land or post. Microscopic examination of wire bonding to through leads shall be made at a minimum magnification of 30X and maximum magnification of 50X with a binocular microscope with the device illuminated with vertical light.

3.1.11.1 Gold wedge and stitch bonds. Bonds shall be entirely within the confines of the package land flat. Reject if the bond is not at least 3/4 of its design size. Rebonds shall not be placed over previous bond attempts.

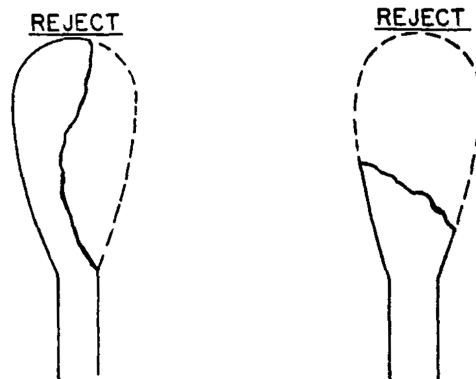

FIGURE 2010-10

3.1.11.2 Gold wire welding. Welds less than 1-1/2 or greater than 3 wire diameters shall be cause for rejection.

3.1.11.3 Aluminum wire bonding. Bonds shall be entirely within the confines of the package land flat and shall be between 1.2 and 3.0 wire diameters or they shall be cause for rejection. Rebonds shall not be placed over previous bond attempts.

3.1.12 Internal lead wires. Microscopic examination of internal lead wires will be conducted at a minimum magnification of 30X and a maximum magnification of 50X with a binocular microscope, and the device illuminated with vertical light.

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METHOD 2010 - Continued

3.1.12.1 Defectives. Any device exhibiting any of the following faults shall be rejected (see figure 2010-11):

(a) Wire loops greater than three times the diameter of the bonding wire when viewed from the top.
(b) Nicks, cuts, crimps or scoring of the bonding wire which reduce the wire diameter by 25%.
(c) Neck down of the bonding wire caused by excessive lead tension which reduces the diameter by 25%.
(d) Extra lead wires or lead tails of more than 3.0 mils in length.
(e) Leads that are closer than 2.0 mils to each other at any point along their length after a distance of 10 mils from the wire to chip bond.
(f) For gold nail head bonded devices the lead wire shall be approximately perpendicular to the surface of the chip for a distance of greater than 0.5 mils before bending toward the package through lead.

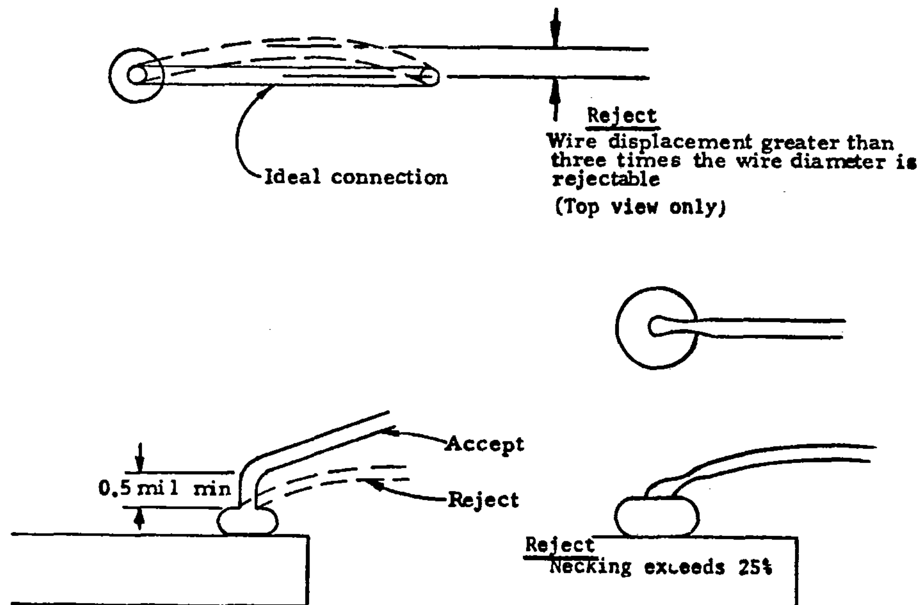

FIGURE 2010-11

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METHOD 2010 - Continued

3.1.13 Chip bonding. Microscopic examination of the chip to header bonding shall be performed at a minimum magnification of 30X and a maximum magnification of 50X utilizing a binocular microscope.

3.1.13.1 Chip orientation. The chip shall be oriented in accordance with the applicable assembly drawing of the device. The orientation will be such that no lead wires cross each other nor any lead wire is closer than 2.0 mils to a second lead wire or to a bonding pad, or to a package through lead. Chip to header melt shall be visible around at least two sides of the chip, excessive melt which is not in accordance with approved processing procedures shall be cause for rejection.

3.1.14 Package condition. Microscopic inspection of the package condition shall be made at a minimum magnification of 30X and a maximum magnification of 50X utilizing a binocular microscope. The general package condition shall be clean and free of any material which could possibly become detached during testing or use.

3.2 Test condition B. Alternate procedure for monolithic and multi-chip microcircuits. Internal visual examination prior to capping or encapsulation shall be conducted on all monolithic and multi-chip microcircuits and all similar devices which are employed in hybrid microcircuit types. The order of examination required in 3.2.1 through 3.2.10 may be varied at the discretion of the manufacturer. All examinations shall be conducted at the specified magnification, with a binocular microscope and the device illuminated with vertical light. All references herein to silicon oxide shall also apply to any other passivation material used in fabricating monolithic and multi-chip microcircuits.

3.2.1 Scratches, missing metallization (80X to 100X). No scratches shall be acceptable in the interconnecting metallization which reduce the width of the conducting stripe by three-fourths or more of the minimum design width, provided the scratch exposes silicon oxide at any point along its length. Scratches, exposing silicon oxide, occurring in metallization contact cut areas shall not be acceptable if they leave three-fourths or more of the contact area isolated from the metallization. Scratches, exposing oxide and occurring on metallization bonding pads shall not be acceptable if they occur in such a manner as to isolate three-fourths or more of the ball bond from the metallization. Missing metallization reducing the width by three-fourths of its narrowest designed width shall be cause for rejection. (See figure 2010-12.)

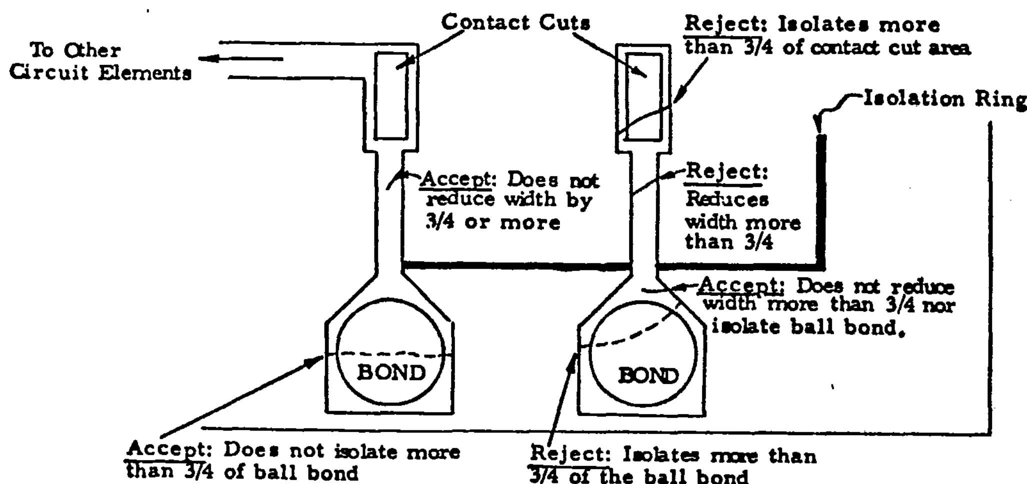

FIGURE 2010-12

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METHOD 2010 - Continued

3.2.2 Bridged metallization (80X to 100X). Reject all material on which silicon oxide is not visible between metallization stripes. Such reductions may be caused by smears, photolithographic defects or conductive foreign material (see figure 2010-13).

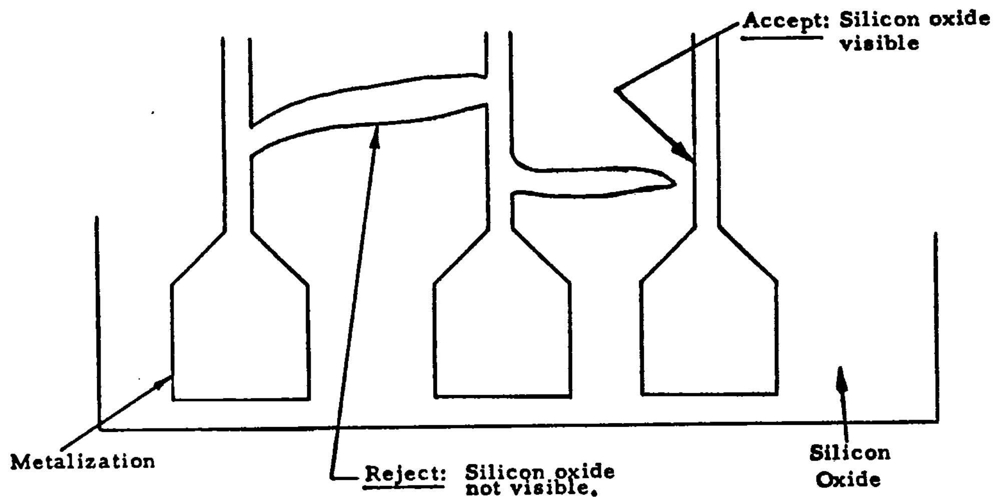

FIGURE 2010-13

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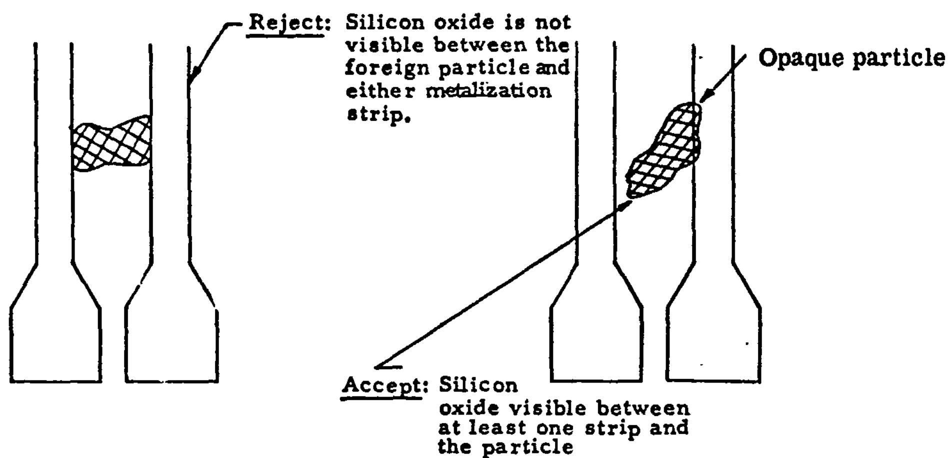
METHOD 2010 - Continued

3.2.3 Foreign material (30X minimum and 50X maximum). Unattached metallic, abrasive or conductive material on the surface of the die or within the package shall not be acceptable. Attached metallic or conductive material shall not be acceptable on the surface of the die if silicon oxide is not visible between the particle and any adjacent metallization. A particle shall be considered attached if it cannot be removed by a nitrogen blow (see figure 2010-14). Conductive foreign material is defined as any opaque substance.



Foreign material

FIGURE 2010-14

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METHOD 2010 - Continued

3.2.4 Cracks (30X minimum and 50X maximum). Same as the high reliability, class "A" requirements as specified in 3.1.7c herein.

3.2.5 Bonding at package land or post (30X minimum and 50X maximum). Bonds not entirely within the confines of the package land flat shall be rejected.

3.2.6 Chip mounting (30X minimum and 50X maximum). The chip shall be properly oriented in accordance with the applicable assembly drawing.

3.2.7 Bond placement (30X minimum and 50X maximum). Devices containing bonds where less than 50 percent of the bond is within the metallization pad area shall be rejected.

3.2.8 Scribed chip (30X minimum and 50X maximum). No chip shall be acceptable if silicon oxide is not visible between each metallization and the scribed edge of the chip (see figure 2010-15).

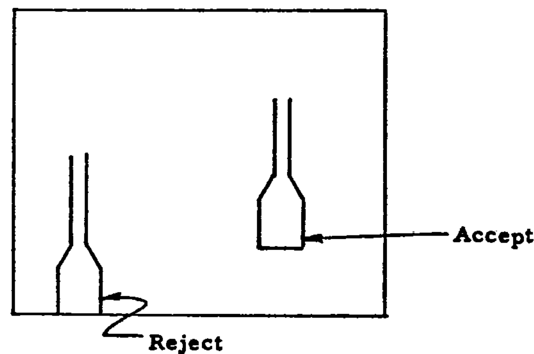

FIGURE 2010-15

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METHOD 2010 - Continued

3.2.9 Internal lead wire tension (30X minimum and 50X maximum). Any loop displaced more than four times the wire diameter when viewed from the top shall be cause for rejection. Wire tension causing necking greater than 50% shall be cause for rejection (see figure 2010-16).

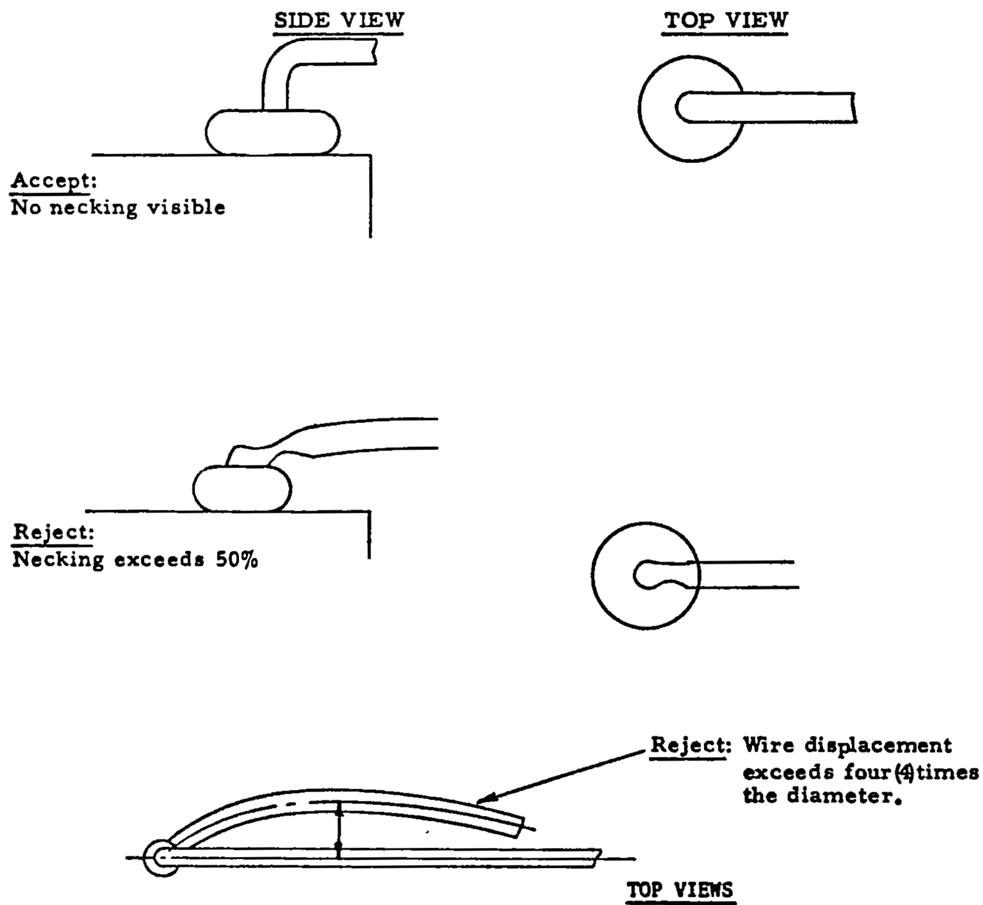

FIGURE 2010-16

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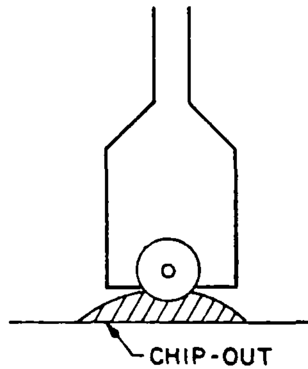
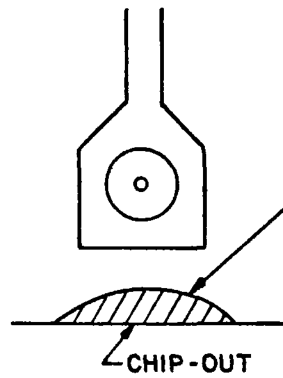
METHOD 2010 - Continued

3.2.10 Chip-out (30X minimum and 50X maximum). No chip-out shall be acceptable unless undisturbed silicon oxide is visible between the metallization and the edge of the chip-out. No chip-out shall be acceptable which appears in the active circuit area (see figure 2010-17).





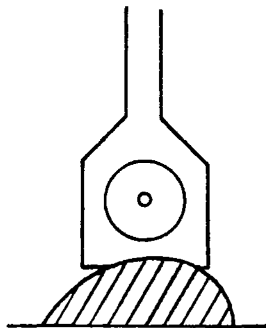


FIGURE 2010-17

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METHOD 2010 - Continued

3.3 Test condition C. Procedure for hybrid microcircuits. An internal visual examination prior to capping or encapsulation shall be conducted on all film hybrid microcircuits. The order of examination required in 3.3.1 through 3.3.14 may be varied at the discretion of the manufacturer. All examinations shall be conducted at the specified magnification. All references herein to substrate shall include all materials used as a base for thin or thick films.

3.3.1 Metallization defects. Microscopic examination for metallization defects shall be made at a minimum magnification of 80X with a binocular microscope and the device illuminated with vertical light. Metallization defects are defined as scratches and/or corrosion and/or voids and/or bridged metallization in the interconnecting metallization patterns of hybrid microcircuits. The rejection criteria for microcircuits with metallization defects are:

(a) A scratch or void in the interconnecting metallization which reduces the width of the conducting stripe to less than one half (1/2) of the minimum designed width, provided the scratch exposes the substrate at any point along its length. (See figure 2010-18.)
(b) Any scratch or void in the metallization, over the dielectric of a capacitor that exposed the underlying dielectric. (See figure 2010-18.)
(c) A scratch or void in the bonding pad metallization if the scratch isolated more than one half (1/2) of the bond from the metallization stripe or a scratch in the bonding pad area which reduces the width of the metallization, in front of the bond toward the active region of the circuit, to less than one half (1/2) of the narrowest design width of the interconnecting metallization (see figure 2010-18).
(d) Any scratch or void at or over a dielectric step (see figure 2010-18).
(e) A scratch that completely crosses a metallization stripe where the substrate is visible at any point along the scratch.
(f) Any evidence of excessive ragged edges, poor adhesion or lifting and discoloration.
(g) Any scratch in the area where contact is made between a film resistor and the interconnect that reduces the conducting path by greater than 25% (see figure 2010-18).

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METHOD 2010 - Continued

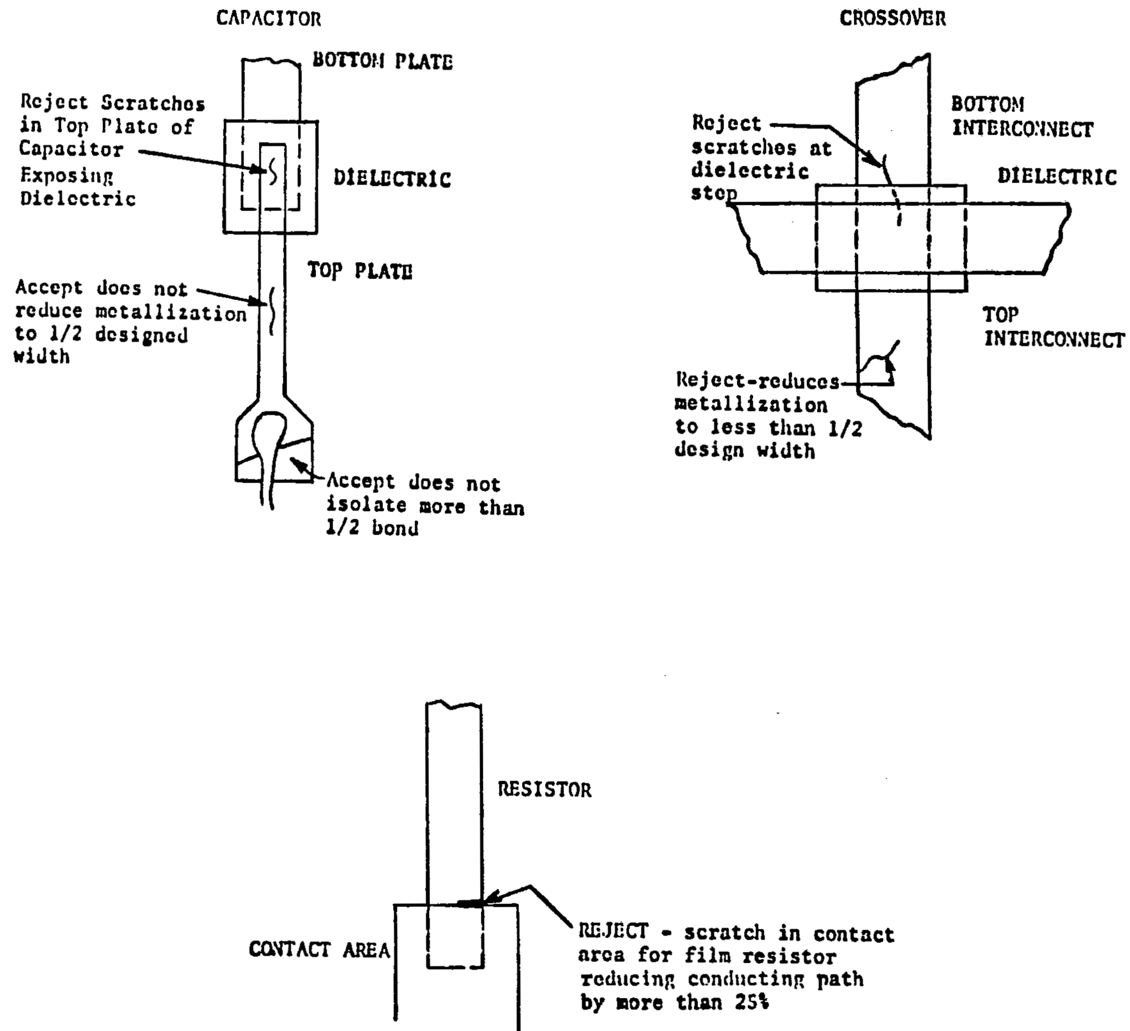

FIGURE 2010-18

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METHOD 2010 - Continued

3.3.2 Corrosion. Microscopic examination for corrosion will be conducted at a minimum magnification of 80X, and will be performed with a binocular microscope with the device illuminated with vertical light.

3.3.2.1 Corrosion defects. Any device with any evidence of corrosion of the metallization will be rejected.

3.3.3 Bridged metallization. Microscopic examination for bridged metallization will be conducted at a minimum magnification of 80X with a binocular microscope and the device illuminated with vertical light.

3.3.3.1 Bridged metallization defects. Any device which exhibits bridged metallization defects to the extent that the distance between any two metallization stripes has been reduced to one quarter (1/4) of the designed separation shall be rejected. This bridging may be caused by smears or photolithographic defects. (See figure 2010-19.)

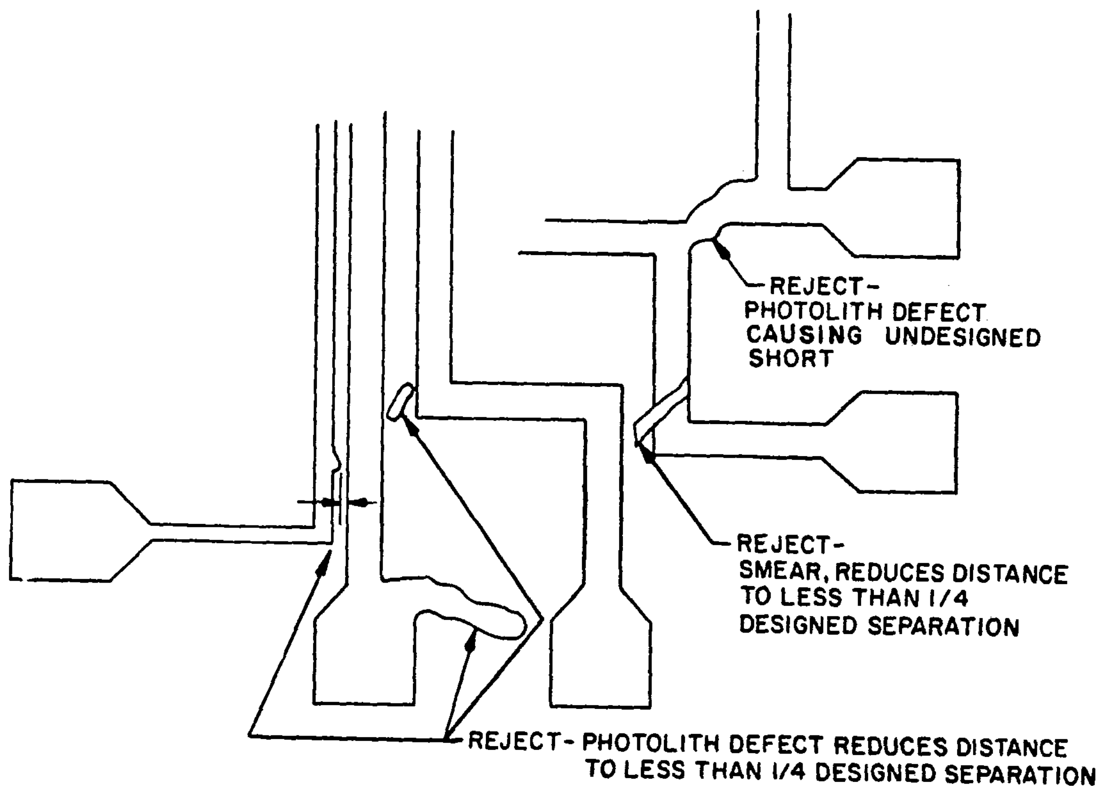

FIGURE 2010-19

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METHOD 2010 - Continued

3.3.4 Metallization alignment. Microscopic examination of the metallization alignment will be made at a minimum magnification of 80X with a binocular microscope and the device illuminated with vertical light.

3.3.4.1 Resistor alignment. Any device in which the metallization does not cover the entire width of a resistor shall be rejected (see figure 2010-20).

3.3.4.2 Capacitor alignment. Any device in which the capacitor dielectric does not completely overlap the bottom metallization plate shall be rejected (see figure 2010-21). Any device in which the region of overlap between the top and bottom metallization plates is not completely separated by dielectric shall be rejected.

3.3.4.3 Crossover alignment. Any device in which the dielectric is not visible between the levels of metallization shall be rejected (see figure 2010-22).

3.3.5 Substrate.

3.3.5.1 Substrate inspection. Microscopic inspection of each substrate will be conducted at a minimum magnification of 80X with a binocular microscope and the device illuminated with vertical light.

(a) Any device which does not have 20 mils separation between the metallization and/or ball bond periphery and the edge of the substrate shall be rejected (see figures 2010-23 and 2010-24).
(b) Any device with chip-outs of the substrate in the active circuit areas shall be rejected.

3.3.6 Cracks. Any device with a crack in the substrate that exceeds 1 mil in length and points toward an active area, metallization or bond shall be rejected. Any device with cracks in the active circuit area or in the metallization pad area shall be rejected (see figure 2010-25).

3.3.7 Resistor faults. Microscopic inspection for resistor faults shall be performed at a minimum magnification of 80X with a binocular microscope and with the device illuminated with vertical light.

(a) Reject any device which has a scratch in the film resistor (see figure 2010-24).
(b) The protective overcoat shall completely cover resistive material or it shall be rejected.

3.3.8 Capacitor and crossover faults. Microscopic inspection for capacitor and crossover faults shall be performed at a minimum magnification of 80X with a binocular microscope and with the device illuminated with vertical light.

(a) Reject any device in which the dielectric has visible bumps, pits, or scratches.

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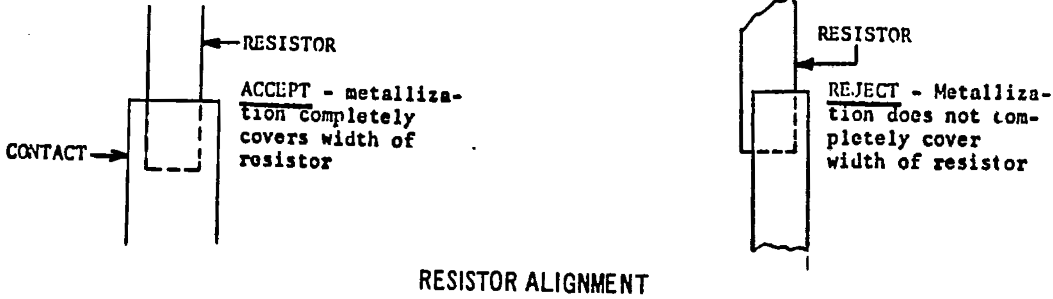
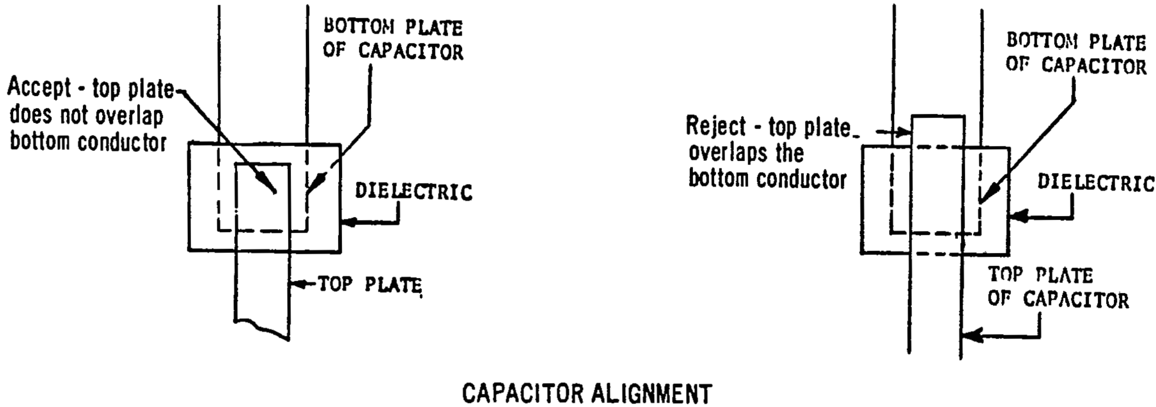
METHOD 2010 - Continued



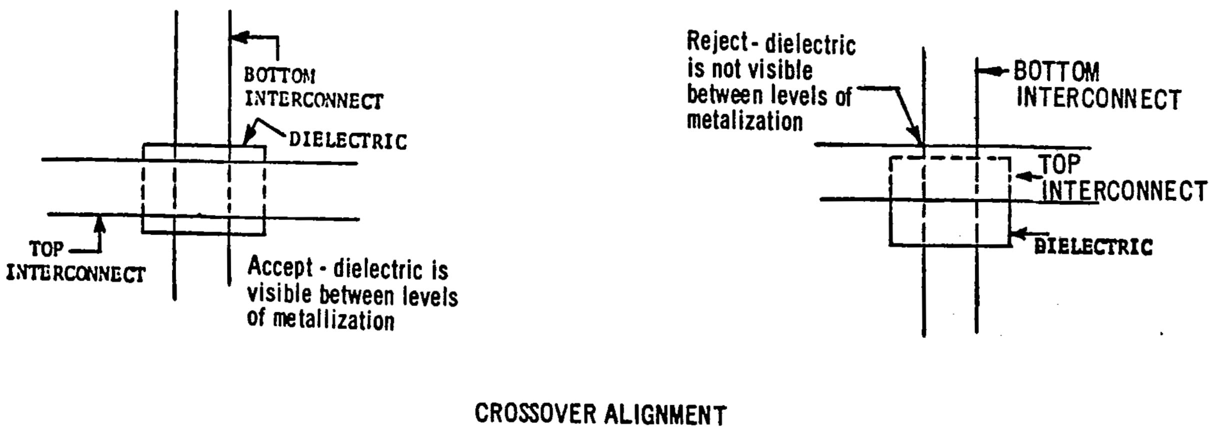
RESISTOR ALIGNMENT

FIGURE 2010-20



CAPACITOR ALIGNMENT

FIGURE 2010-21



CROSSOVER ALIGNMENT

FIGURE 2010-22

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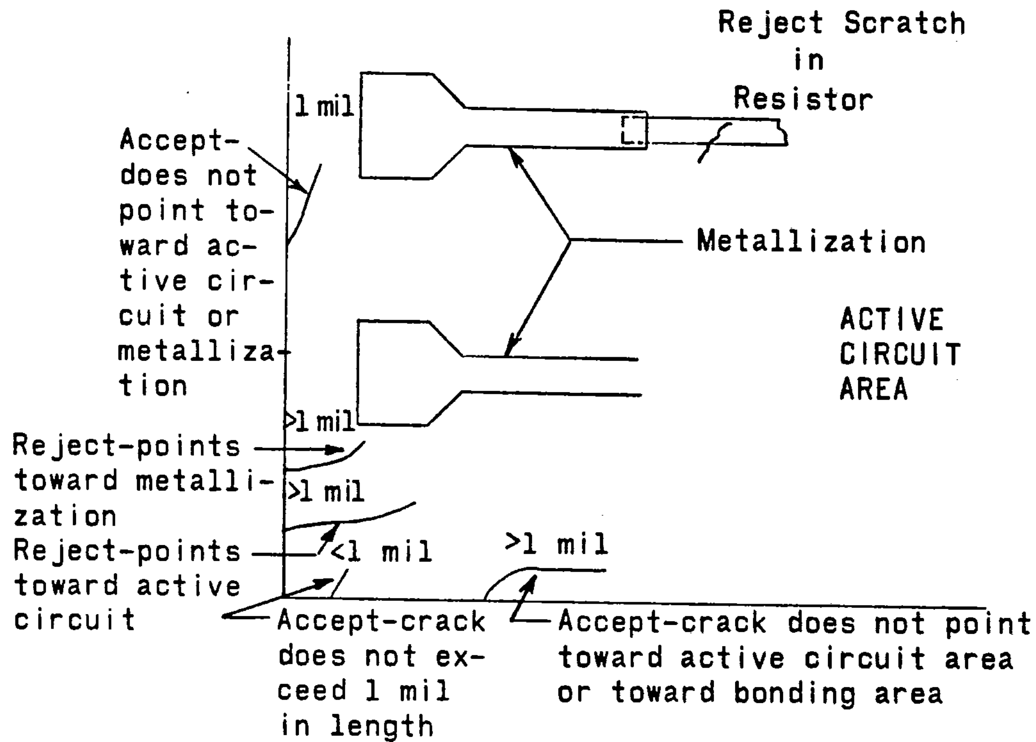
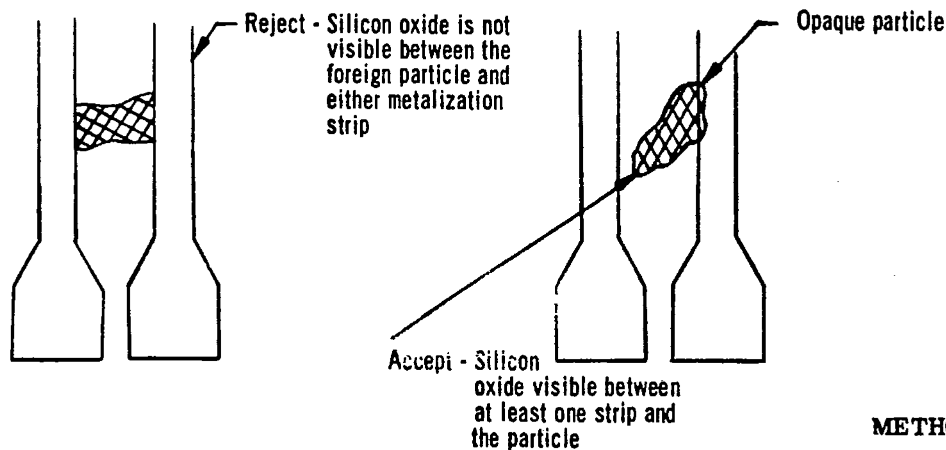
METHOD 2010 - Continued



CRACK REJECTION CRITERIA

FIGURE 2010-25A



FOREIGN MATERIAL

FIGURE 2010-25B

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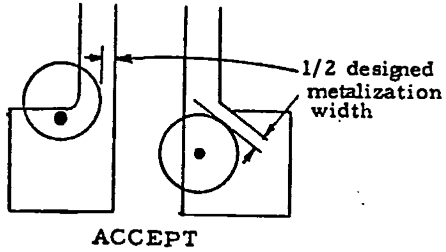
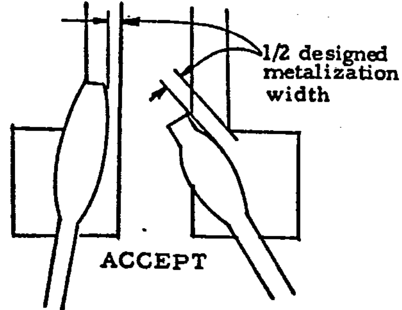
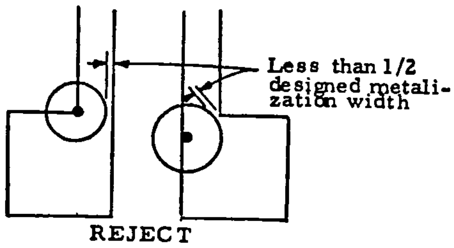
METHOD 2010 - Continued

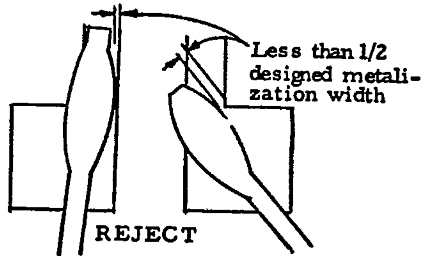
BALL BONDS

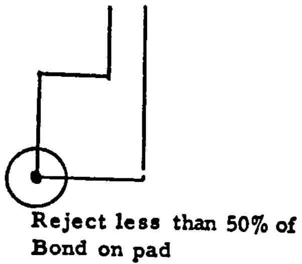
ULTRASONIC BONDS

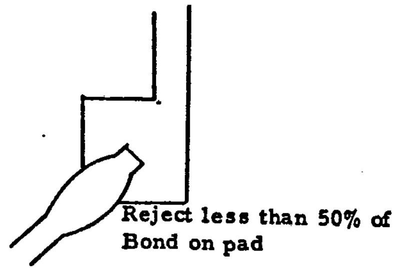


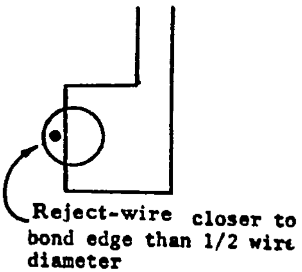












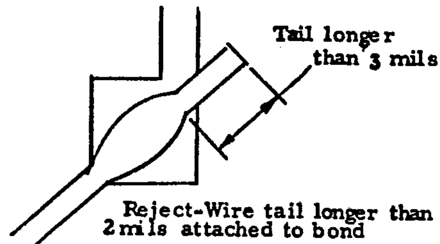


FIGURE 2010-26

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METHOD 2010 - Continued

FIGURE 2010-27

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METHOD 2010 - Continued

3.3.11 Bonding at package land or post. Microscopic examination of wire bonding to through leads shall be made at a minimum magnification of 30X and a maximum magnification of 50X with a binocular microscope with the device illuminated with vertical light.

(a) Gold wedge and stitch bonds. Bonds shall be entirely within the confines of the package land flat. Reject if the bond is not at least 3/4 its design size.
(b) Gold wire welding. Welds less than 1-1/2 or greater than three wire diameters shall be cause for rejection.
(c) Aluminum bonding. Bonds shall be entirely within the confines of package land flat and shall be between 1.2 and 3.0 wire diameters or they shall be cause for rejection. Rebonds shall not be placed over previous bond attempts.

3.3.12 Internal lead wires. Microscopic examination of internal lead wires will be conducted at a minimum magnification of 30X and a maximum magnification of 50X with a binocular microscope.

3.3.12.1 Defectives. Any device exhibiting any of the following faults shall be rejected:

(a) Wire loops greater than three times the diameter of the bonding wire when viewed from the top.
(b) Nicks, cuts, crimps or scoring of the bonding wire which reduce the wire diameter by 25%.
(c) Neck down of the bonding wire caused by excessive lead tension which reduces the diameter by 25%.
(d) Extra lead wires or lead tails of more than 3.0 mils in length.
(e) Leads that are closer than 2.0 mils to each other at any point along their length, after a distance of 10 mils from the wire to substrate bond.
(f) For gold nail head bonded devices to the lead wire shall be approximately perpendicular to the surface of the substrate for a distance of 0.5 mils before bending toward the package through lead.

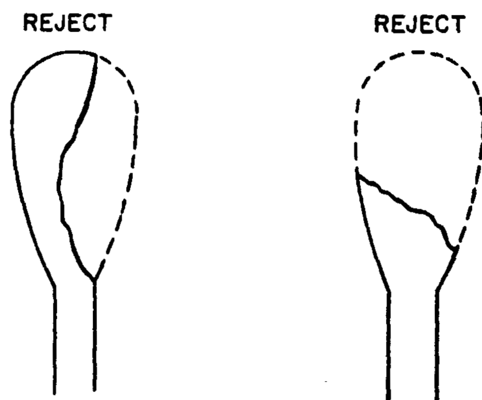

FIGURE 2010-28

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METHOD 2010 - Continued

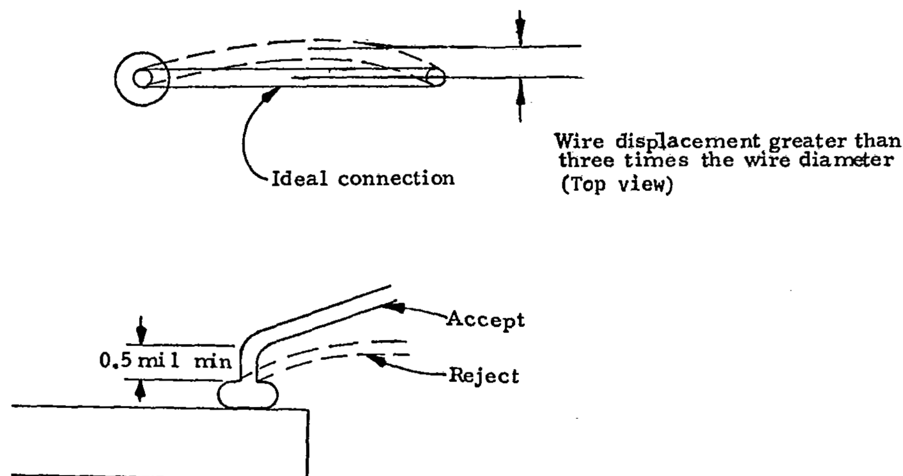

FIGURE 2010-29

3.3.13 Substrate bonding. Microscopic examination of the substrate to header bonding shall be performed at a minimum magnification of 30X and a maximum magnification of 50X utilizing a binocular microscope.

(a) The substrate shall be oriented in accordance with the applicable assembly drawing of the device. The orientation will be such that no lead wires cross each other nor any lead wire is closer than 2.0 mils to a second lead wire or to a bonding pad, or to a package through lead. Substrate to header melt shall be visible around at least two sides of the substrate, excessive melt which is not in accordance with approved processing procedures shall be cause for rejection.

3.3.14 Package condition. Microscopic inspection of the package condition shall be made at a minimum magnification of 30X and a maximum magnification of 50X.

(a) The general package condition shall be clean and free of any material which could possibly become detached during testing or use.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition (see 3).
(b) Where applicable, any exceptions or modifications to the specified procedure and criteria.
(c) Where applicable, gages, drawings and photographs to be used as standards for operator comparison (see 2).

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METHOD 2011

BOND STRENGTH

1. PURPOSE. The purpose of this test is to destructively measure bond strengths, evaluate bond strength distributions or determine compliance with specified bond strength requirements of the applicable procurement document as specified in device qualification or lot acceptance requirements. This test may be applied to the wire to die bond or the wire to package lead bond inside the package of wire-connected microelectronic devices bonded by soldering, thermocompression, ultrasonic or related techniques. It may also be applied to bonds external to the device such as those from device terminals to substrate or wiring board or to internal bonds between die and substrate in face-bonded device configurations.

2. APPARATUS. The apparatus for this test shall consist of suitable equipment for applying the specified stress to the bond, lead wire or terminal as required in the specified test condition. A calibrated measurement and indication of the applied stress in grams at the point of failure shall be provided by the equipment capable of measuring stresses up to and including 10 grams with an accuracy of $^{+0}_{-0.5}$ grams, stresses between 10 and 50 grams with an accuracy of $^{+0}_{-1}$ grams and stresses exceeding 50 grams with an accuracy of $^{+0}_{-5}$ percent of indicated value.

3. PROCEDURE. The test shall be conducted in accordance with the specified test condition to determine compliance with the requirements of the applicable procurement document. The stress required to achieve bond failure shall be observed and the physical location of the point of failure shall be recorded as being in one of the following categories:

(a) For internal bonds connecting chip or substrate to lead frame:

(1) Wire break at neckdown point (reduction of cross section due to bonding process).
(2) Wire break at point other than neckdown.
(3) Failure in bond (interface between wire and metallization).
(4) Lifted metallization (separation of metallization of bonding pad from die or substrate).
(5) Fracture of die or substrate (removal of portion of substrate immediately under the bond).

(b) For external bonds connecting device to wiring board or substrate:

(1) Lead or terminal break at deformation point (weld affected region).
(2) Lead or terminal break at point not affected by bonding process.
(3) Failure in bond interface (in solder or at point of weld interface between lead or terminal and the board or substrate conductor to which the bond was made).
(4) Conductor lifted from board or substrate.
(5) Fracture within board or substrate.

(c) For face-bonded configurations:

(1) Failure in the bond material or pedestal, if applicable.
(2) Fracture of die (or carrier) or substrate (removal of portion of die or substrate immediately under the bond).
(3) Lifted metallization (separation of metallization or bonding pedestal from die (or carrier) or substrate.

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METHOD 2011 - Continued

3.1 Test condition A. Bond peel. This test is normally employed for bonds external to the device package. The lead or terminal and the device package shall be gripped or clamped in such a manner that a peeling stress is exerted with the specified angle between the lead or terminal and the board or substrate. Angles of 30, 45, and 90° only shall be specified and where no angle is specified in the individual specification, an angle of 90° shall be used. The force required to cause failure and the failure category shall be recorded.

3.2 Test condition B. Bond shear. This test is normally employed for internal bonds at the die or substrate and the lead frame of microelectronic devices. A suitable tool or wedge shall be brought in contact with the wire and bond at a point just above the die or substrate metallization and a force applied parallel to the substrate, to cause bond failure by shear. The tool shape shall be such as to cause a minimum of cutting action at the tool edge so that the force is applied across the entire bond interface. The force required to cause failure and the failure category shall be recorded.

3.3 Test condition C. Wire pull (single bond). This test is normally employed for internal bonds at the die or substrate and the lead frame of microelectronic devices. The wire connecting the die or substrate shall be cut so as to provide two ends accessible for pull test. In the case of short wire runs, it may be necessary to cut the wire close to one termination in order to allow pull test at the opposite termination. The wire shall be gripped in a suitable device and simple pulling action applied to the wire or to the device (with the wire clamped) in such a manner that the force is applied normal to the surface of the die or substrate. The force required to cause failure and the failure category shall be recorded.

3.4 Test condition D. Wire pull (double bond). This procedure is identical to that of test condition C, except that the pull is applied by inserting a hook under the lead wire (attached to die, substrate or header at both ends) with the device clamped and the pulling force applied normal to the die or substrate surface. In this test condition the actual force at the bond is other than normal to the die or substrate and additional ambiguity is provided by the fact that two bonds are tested simultaneously allowing measurement of only the weakest bond or section of wire in the loop. The force required to cause failure and the failure category shall be recorded.

3.5 Test condition E. Gas blast. This test is normally employed for internal bonds at the die or substrate and the lead frame of microelectronic devices. Stress is applied approximately parallel to the die or substrate surface by directing a concentrated blast of air or gas across the surface and against the lead wire and bond. This test condition is ambiguous and is difficult to calibrate in terms of a specific stress to failure. It shall be used only as an in-line screen to detect weak bonds or bonds with strengths below some nominal strength level. The level of correlation shall be determined by calibrating the gas blast procedure against the more specific procedure of test conditions A, B, or C.

3.6 Test condition F. Bond shear (flip chip). This test is normally employed for internal bonds between a semiconductor die and a substrate to which it is attached in a "flip-chip" or face-bonded configuration. It may also be used to test the bonds between a substrate and an intermediate carrier or secondary substrate to which the die is mounted. A suitable tool or wedge shall be brought in contact with the die (or carrier) at a point just above the primary substrate and a force applied perpendicular to one edge of the die (or carrier) and parallel to the primary substrate, to cause bond failure by shear. The force required to cause failure, the number of bonds per die (or carrier) involved in the individual device design, and the failure category shall be recorded.

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METHOD 2011 - Continued

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test condition letter (see 3).
(b) Minimum bond strength or details of specified strength distributions if applicable.
(c) Number and selection of bonds to be tested on each device, and number of devices. Unless otherwise specified all bonds on the device shall be tested in accordance with the specified test condition.
(d) For test condition A, angle of bond peel (see 3.1).
(e) For test condition E, details of nozzle design, nozzle placement with reference to the device, type of gas, and flow rate (or pressure through a calibrated nozzle) (see 3.5).

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METHOD 2012

RADIOGRAPHY

1. PURPOSE. The purpose of this examination is to detect defects within the sealed case, especially those resulting from sealing of the lid to the case and internal defects such as foreign objects, improper interconnecting wires and voids in the die counting material or in the glass, when glass seals are used.

2. APPARATUS. The apparatus and materials for this test shall include:

(a) Radiographic equipment with a voltage range up to 100 KV, a focal spot of 1.5 mm or less, and a focal film distance sufficient to produce the required image.
(b) Radiographic film - Very fine grain film, with 0.001 inches resolution.
(c) Radiographic viewer - Capable of 0.001 inches resolution in major dimension.
(d) Holding fixtures - Capable of holding devices in the required positions without interfering with the accuracy or ease of image interpretation.

3. PROCEDURE.

3.1 Mounting. The devices shall be mounted in the holding fixture in such a manner that the devices are not damaged or contaminated and are in the proper plane as specified.

3.2 Radiographic quality standard. Each radiographic shall have a radiographic quality standard located (and properly identified) at the point on the film most remote from the central X-ray beam. The radiographic quality standard shall consist of a device, the same or similar in materials and construction as those to be tested, with defects intentionally placed within the device. Type and size of defects shall be as established by the manufacturer's quality assurance activity and approved by the contracting agency. A typical "standard" would be prepared from a sealed device having one broken internal interconnecting wire (0.001 inch diameter maximum) and one solder particle (0.001 inch maximum in any dimension) within the device. Both defects shall be clearly visible on the radiograph when viewed at 7X magnification. A radiographic quality standard such as ASTM type B - Image quality indicator for semiconductor radiography or equivalent device may be used. Two quality standards shall be exposed with each view, placed in opposite corners of the film.

3.3 Film and marking. The radiographic film shall be in a film holder backed with a minimum of 1/16 inch lead. The film shall be identified with punched lead foil or lead characters and shall include at least the following information:

(a) Device manufacturer's name or code identification number.
(b) Device type or part number.
(c) Production lot number or date code or inspection lot number.
(d) Radiographic film view number and date.

3.3.1 Non-film techniques. The use of non-film techniques is permitted if permanent records are not required and the equipment is capable of producing results of equal quality when compared to film techniques, and all requirements of this method are complied with except those pertaining to the actual film.

3.4 Tests. The X-ray equipment shall be adjusted for the proper voltage, focal spot, and film distance and the device shall be "shot" for the predetermined time interval required to produce acceptable radiographs. Radiographs shall be made for each view required (see 4).

3.5 Processing. The radiographic film manufacturer's recommended procedures shall be used to develop the exposed film.

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METHOD 2012 - Continued

3.6 Operating personnel. Personnel who will perform radiographic inspection shall have training in radiographic procedures and techniques so that defects revealed by this method can be validly interpreted and compared with applicable standards. The following minimum vision requirements shall apply for visual acuity of personnel inspection film:

(a) Distant vision shall equal at least 20/30 in both eyes, corrected or uncorrected.
(b) Near vision shall be such that the operator can read Jaeger type No. 2 at a distance of 16 inches, corrected or uncorrected.
(c) Vision tests shall be performed by an oculist, optometrist or other professionally recognized personnel at least once a year. Personnel authorized to conduct radiographic tests shall be required to pass the vision tests specified in (a) and (b).

3.7 Interpretation of radiographs. Interpretation of the radiograph shall be made under low light level conditions without glare on the radiographic viewing surface. An illuminator such as General Electric Model CO, type 2, or equivalent, shall be used. The radiograph shall be viewed at a magnification between 6X and 8X. Questionable defects may be examined under higher magnification, as specified. Viewing masks may be used when necessary. Any radiograph not clearly illustrating the defects in the radiographic quality standard is not acceptable and another radiograph of the devices shall be taken.

3.8 Protection of radiographs. A radiograph of each device processed (including defective devices) shall be placed in protective containers, properly identified and either shipped with the devices or placed on file as specified.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) What view(s) of the device shall be taken.
(b) Disposition of radiographs (see 3.8).
(c) Marking if other than indicated in 3.3 and marking of samples to indicate they have been radiographed, if required.
(d) Defects to be sought in the samples and criteria for acceptance or rejection.

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METHOD 2013

INTERNAL VISUAL

1. PURPOSE. The purpose of this destructive test is to examine those devices opened for post test evaluation to determine if they show any evidence of corrosion, poor bonding, other defects or damage resulting from prior testing.

2. APPARATUS. The apparatus required for the performance of this test shall include a binocular microscope capable of 80X to 100X magnification and both light and dark field illumination and any visual or mechanical standards to be used for measurement or comparison.

3. PROCEDURE. The device shall have the lid removed by a technique which does not damage or contaminate the internal structure or in any way impair the ability to observe defects in the devices or the effects of preceding test exposures. The device shall be examined with a binocular microscope utilizing vertical illumination at a minimum magnification of 80X to determine the existence of any visual defects. Particular attention shall be given to corrosion, metallization peeling, foreign materials, substrate cracks, chemical formations and intermetallic reactions. Where bonds are removed, the bonding pads shall be carefully examined for evidence indicating poor bonding such as cleavage under the bond, insufficient or excessive bonding pressure or temperature and intermetallic formation.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Test conditions (see 3).
(b) Where applicable, any additions or modifications to the specified procedure and criteria.
(c) Where applicable, gages, drawings, and photographs to be used as standards for the operator comparison (see 2).

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METHOD 3001

DRIVE SOURCE, DYNAMIC

1. PURPOSE. This method establishes a drive source to be used in measuring dynamic performance of logic gating circuits.

2. APPARATUS.

2.1 TTL, DTL. A driving source capable of supplying flat top and bottom signals with rise transistions that are linear from 10% to 80% and fall transitions that are linear from 90% to 20% shall be provided. The impedance of this driving source shall be sufficiently low to maintain signal levels and transition time linearities defined in the applicable procurement document. The driving signal is to be measured at the input terminal of the device under test with the device conditioned according to the applicable procurement document. Particular attention shall be paid to the line used to transmit the driving signal from the driving source to the test circuit input. Large changes in input impedance which may occur as the driving signal traverses the test circuit actuation point could produce line reflections or signal ringing. The driver source shall have controlled frequency, duty factor, signal levels and signal transition times. Ringing and noise at both levels of the signal shall be controlled (0 to peak) to less than 10% of the total signal amplitude. Figure 3001-1 shows the important signal parameters.

2.2 TTL, DTL (alternate driving source). As an alternative driving source, a typical circuit, selected from the same family as the device under test, shall be used as a driving source. This circuit, hereafter referred to as the driving gate, shall have an output rise time as specified in the applicable procurement document. This rise time shall be defined $V_A + 0.1\ (V_{(B)} - V_{(A)})$ to the threshold voltage point (see figure 3001-2) and shall be measured with the device under test removed from the test circuit. The input to the driving gate shall be a source which has an up level of V_{OH} and a down level of 0 volts. In addition, it shall have the following characteristics: t_r and $t_f \leq 15$ nanoseconds, PRF $\geq$ 100 kHz pulse width of negative portion + 1 microsecond at the threshold voltage point. Figure 3001-2 shows a typical test configuration and important signal parameters.

2.3 ECL. The driving source shall be considered the output of a bias driver of input gate driver. The bias driver shall be designed to assure that the threshold point of the circuit under test is always in the center of the transition region as specified in the applicable procurement document, and the input driver shall be selected from the same family as the device under test. The input to the driver shall be a source which has an up level of 0 volts and a down level of V_{OL}. In addition, it shall have the following characteristics: t_r and $t_f \leq 2$ nanoseconds, PRF $\geq$ 100 kHz, pulse width $\geq$ 50 nanoseconds. The input source to the driver should be terminated in its characteristic impedance Zo at the test-jig. Coax cable with the same Zo should be used between the source and the driver to minimize overshoots and undershoots to the driver. Ringing and noise at both levels of the signal shall be controlled (0 to peak) to less than 5% of the total signal amplitude. Figure 3001-3 shows a typical test configuration and important signal parameters.

2.4 RTL. Two typical circuits selected from the same family as the device under test or an appropriate driving circuit shall be used as the driving source. This circuit(s), hereafter referred to as the driving gate, shall have an output rise time as specified in the applicable procurement document. This rise time shall be defined from $V_A + 0.1\ (V_{(B)} - V_{(A)})$ to $V_A + 0.9\ (V_{(B)} - V_{(A)})$ (see figure 3001-4) and shall be measured with the device under test removed from the test circuit. The input to the driving gate shall be a source which has an up-level of V_{OH} and a down level of 0 volts. In addition, it shall have the following characteristics: $t_r \leq 50$ nanoseconds, PRF = 100 kHz, pulse width = 100 nanoseconds. Figure 3001-4 shows two typical test configurations and important signal parameters.

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METHOD 3001 - Continued

3. PROCEDURE.

3.1 TTL, DTL. Using the driving source of 2.1, the transition times, transition linearities, levels, repetition frequency, and duty factor of the driving signal shall be defined in the applicable procurement document. Level V_A shown in figure 3001-1 is critical to t_{pdL} delay and care should be taken to adjust this level to within 20 MV of the specified level with a device under test in the test circuit. Level V_B shall be specified as a nominal V_{OH}. The driving signal shall be measured at the input terminal of the test circuit. The test circuit shall be switched by the driving signal and have normal bias voltages applied.

3.2 TTL, DTL (alternate driving source). Using the alternate driving source of 2.2, signal V_{IN}, shown in figure 3001-2, shall be adjusted to the specified t_r in the applicable procurement document, with the device under test removed from the test circuit. t_r may be adjusted by selecting driving gate circuits or adjusting C_{IN}. Level V_A shall be specified as a nominal V_{OL}. Level V_B shall be specified as a nominal V_{OH}.

3.3 ECL. The output of the bias driver or input gate driver shall be adjusted to the specified t_r and threshold point in the applicable procurement document with the device under test removed from the test circuit. For the bias driver t_r may be adjusted by varying C_{IN} or adjusting the source driving the bias driver and the threshold point is adjusted by varying the bias driver voltage (-V) (see figure 3001-3).

3.4 RTL. The signal V_{IN} shown in figure 3001-4 shall be adjusted to the specified t_r in the applicable procurement document with the device under test removed from the test circuit. Level $V_{(A)}$ shall be specified as a nominal V_{OL} and level $V_{(B)}$ shall be specified as a nominal V_{OH}.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Levels V_A and V_B, where applicable.
(b) Driving signal transition times.
(c) Repetition frequency.
(d) Duty factors.
(e) Driving gate and/or circuit, where applicable.
(f) Bias driver, where applicable.
(g) C_{IN} where applicable.
(h) Specific pulse generator required, if applicable.

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METHOD 3001 - Continued

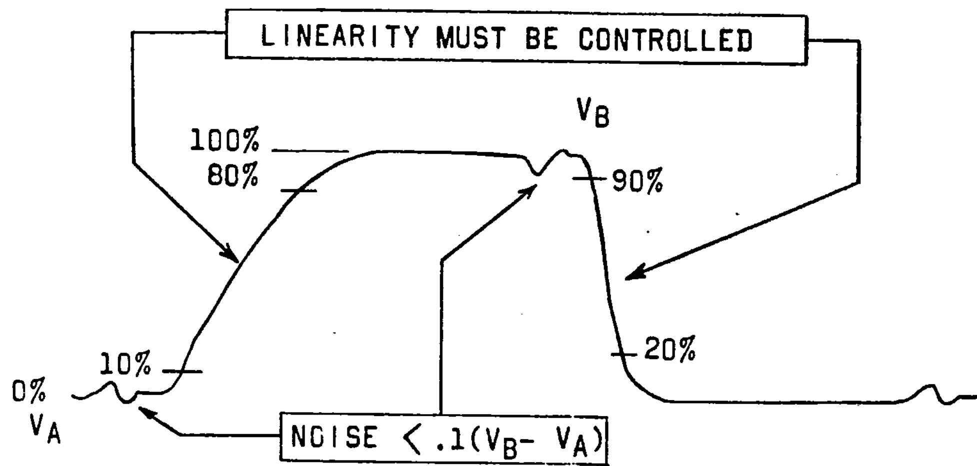

FIGURE 3001-1. Drive signal for TTL, DTL.

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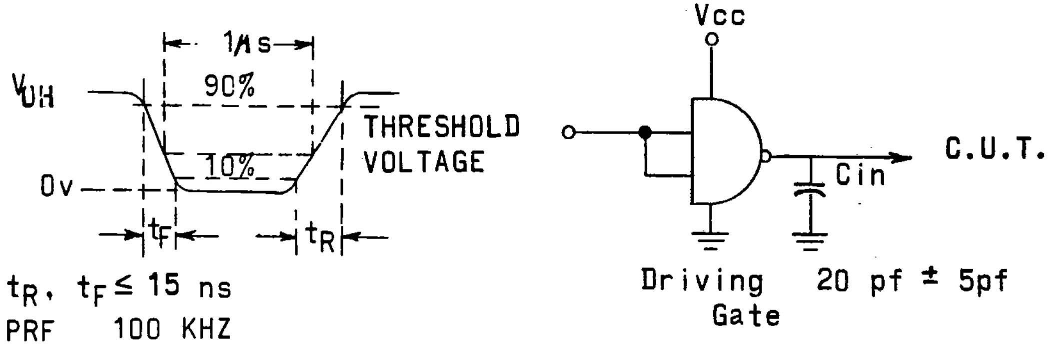
METHOD 3001 - Continued



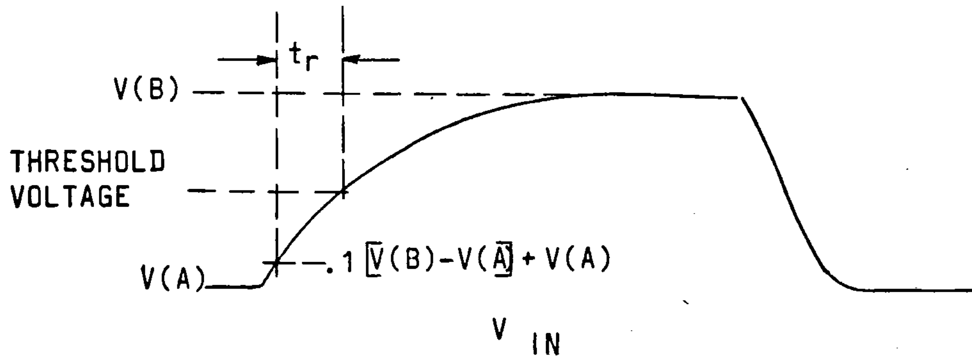


FIGURE 3001-2. Drive signal for DTL, TTL.

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METHOD 3001 - Continued

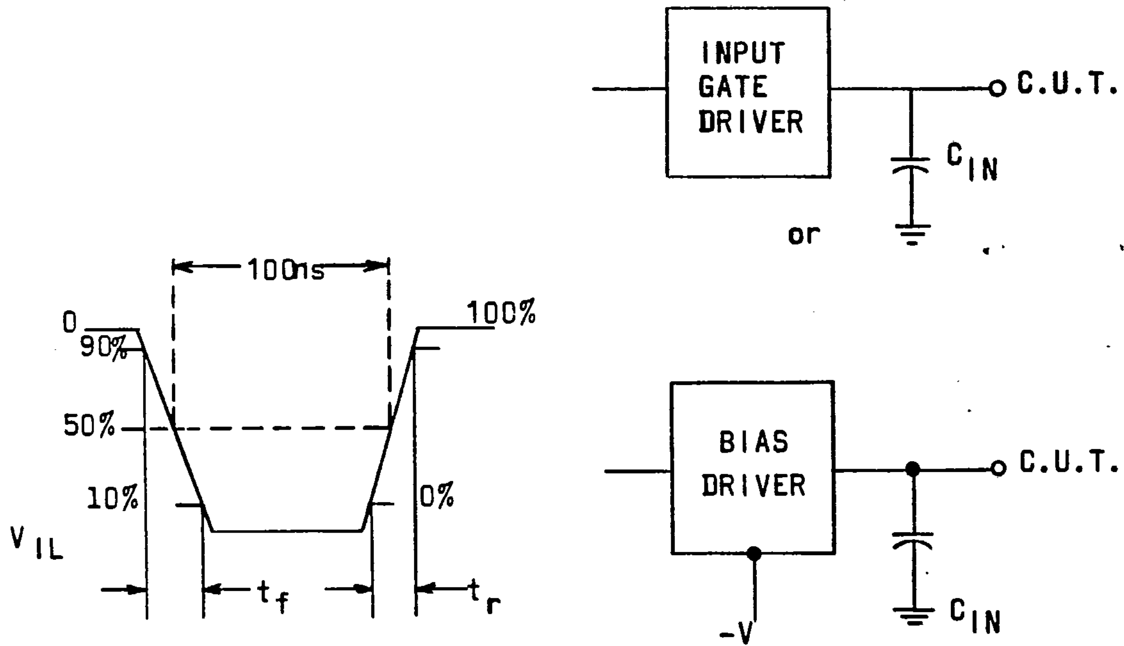

FIGURE 3001-3. Driving source for ECTL.

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METHOD 3001 - Continued

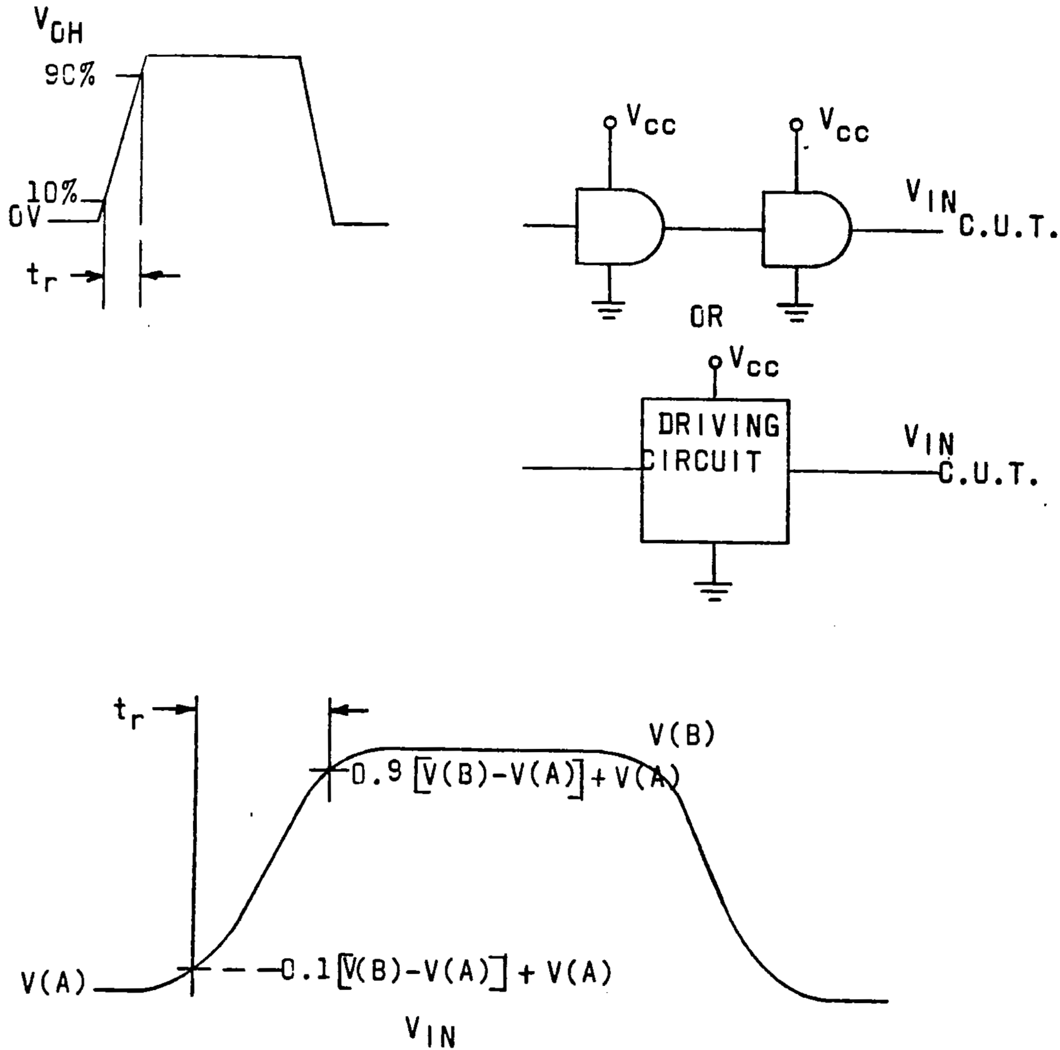

FIGURE 3001-4. Driving source for DTL.

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METHOD 3002

LOAD CONDITIONS

1. PURPOSE. This method establishes the load conditions to be used in measuring dynamic performance of logic gating circuits, such as TTL, DTL, RTL, and ECTL.

2. APPARATUS.

2.1 Simulated load. The load shall simulate the worst case conditions for the circuit parameters being tested. This load will represent the circuit parameters of the normal load as specified in the applicable procurement document.

2.2 Discrete component load. The load will consist of any combination of capacitive, inductive, resistive, or diode components.

2.2.1 Capacitive load (C_L). The worst case load capacitance that the circuit under test can tolerate and still meet the dynamic performance specified shall be used. This will represent the input capacitance of the normal load for the device, the maximum line capacitance, and the probe and test fixture capacitance. The fixed value of capacitance shall be specified in the applicable procurement document.

2.2.2 Inductive (L_L). The worst case load inductance that the circuit under test can tolerate and still meet the dynamic performance specified shall be used. This will represent the input inductance of the normal load for the device, the maximum line inductance, and the probe and test fixture inductance. The fixed value of inductance shall be specified in the applicable procurement document.

2.2.3 Resistive load (R_L). The resistive load shall represent the worst case fan out conditions of the device under test. For sink loads, the resistor shall be connected between V_{CC} and gate output; and for source loads, the resistor shall be connected between gate output and ground.

2.2.4 Diode load (D_L). The diode load shall represent the input diode(s) of the circuit under test. The equivalent diode, as specified in the applicable procurement document, will also represent the base-emitter or base-collector diode of any transistor in the circuit path of the normal load.

2.3 Dynamic load change. The load shall automatically change its electrical parameters as the device under test changes logic state if this is the normal situation for the particular family of circuits being tested. One method of accomplishing this dynamic change is to use devices from the same logic family equal to the worst case fan out as the load.

3. PROCEDURE. The load will normally be paralleled by a high impedance voltage detection indicator. The indicator may be either visual or memory storage.

4. SUMMARY. The following must be defined in the applicable procurement document:

(a) C_L, L_L, R_L, D_L and equivalent circuit (see 2.2).

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METHOD 3003

PROPAGATION DELAY

1. PURPOSE. This method establishes the means for measuring propagation delay of logic gating circuits.

1.1 Definitions. The following definitions for the purpose of this test method shall apply.

1.1.1 Propagation delay (t_{pdL}). The time measured with the specified output changing from the defined high level to the defined low level with respect to the corresponding input transition.

1.1.2 Propagation delay (t_{pdH}). The time measured with the specified output changing from the defined low level to the defined high level with respect to the corresponding input transition.

2. APPARATUS. Equipment capable of measuring elapsed time between the input signal and output signal at the 50% point or any voltage point between the maximum low level and minimum high level shall be provided. The input shall be supplied by a driving source as described in method 3001 of this standard. It is desirable for this equipment to have data logging capability so that circuit dynamic performance distribution can be monitored.

3. PROCEDURE. The test circuit shall be loaded according to method 3002 of this standard. The driving signal to the test circuit shall be provided according to method 3001 of this standard.

3.1 Measurements at a voltage point. t_{pdL} and t_{pdH} shall be measured from the threshold voltage point on the driving signal to the threshold voltage point on the test circuit output signal for both inverting and noninverting logic. These delays shall be measured at the input and output terminals of the device under test. Figure 3003-1 shows typical delay readings.

3.2 Measurements at 50% points. t_{pdL} and t_{pdH} shall be measured from the 50% point on the driving signal to the 50% point on the test circuit output signal for both inverting and noninverting logic. These delays shall be measured at the input and output terminals of the device under test. Figure 3003-2 shows typical delay readings.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) t_{pdL} and t_{pdH} limits.
(b) Parameters of the driving signal.
(c) Load conditions.
(d) Conditioning voltages.
(e) Measurement points (see 3.1 and 3.2).

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METHOD 3003 - Continued

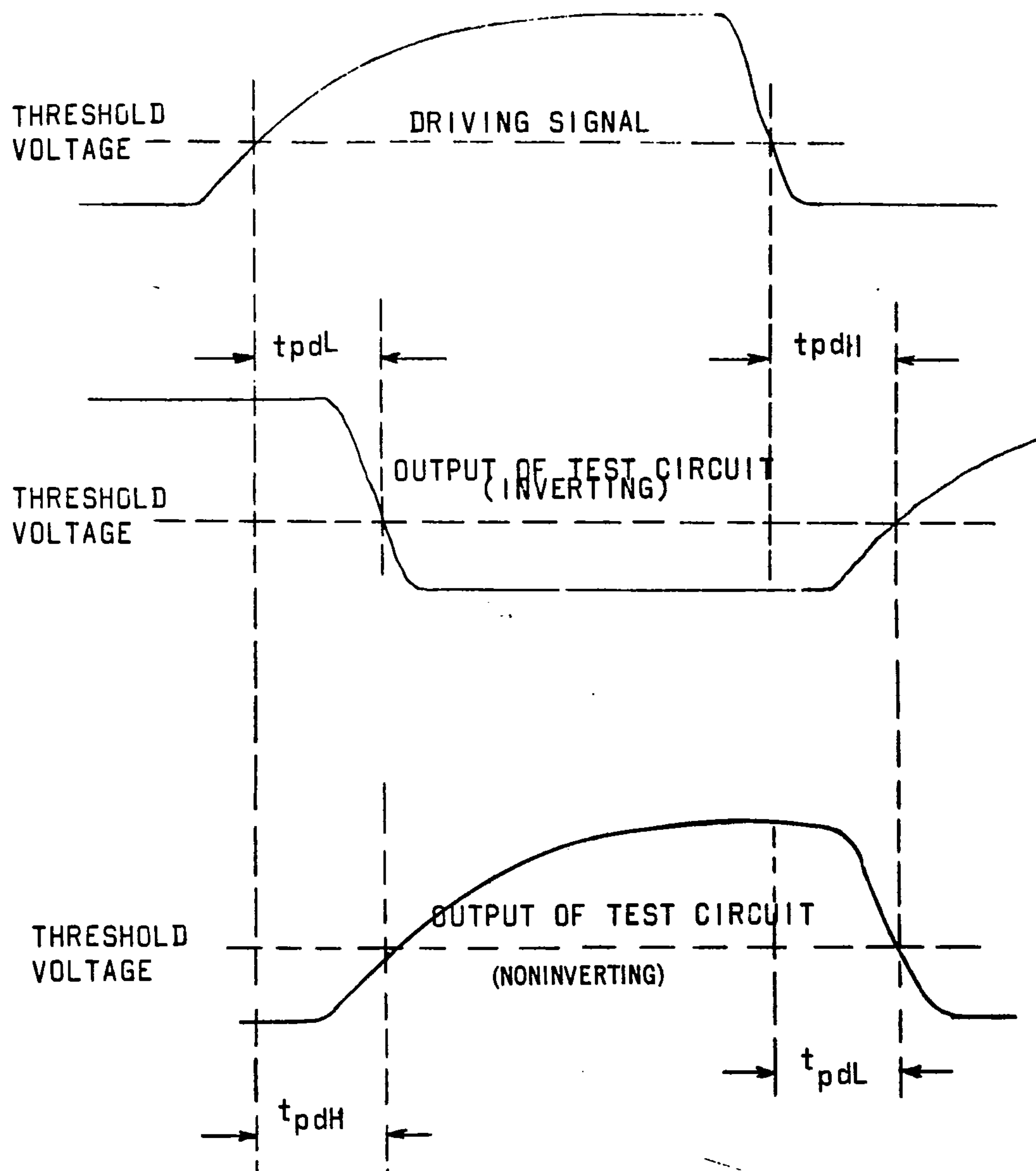

FIGURE 3003-1. Propagation delay.

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METHOD 3003 - Continued

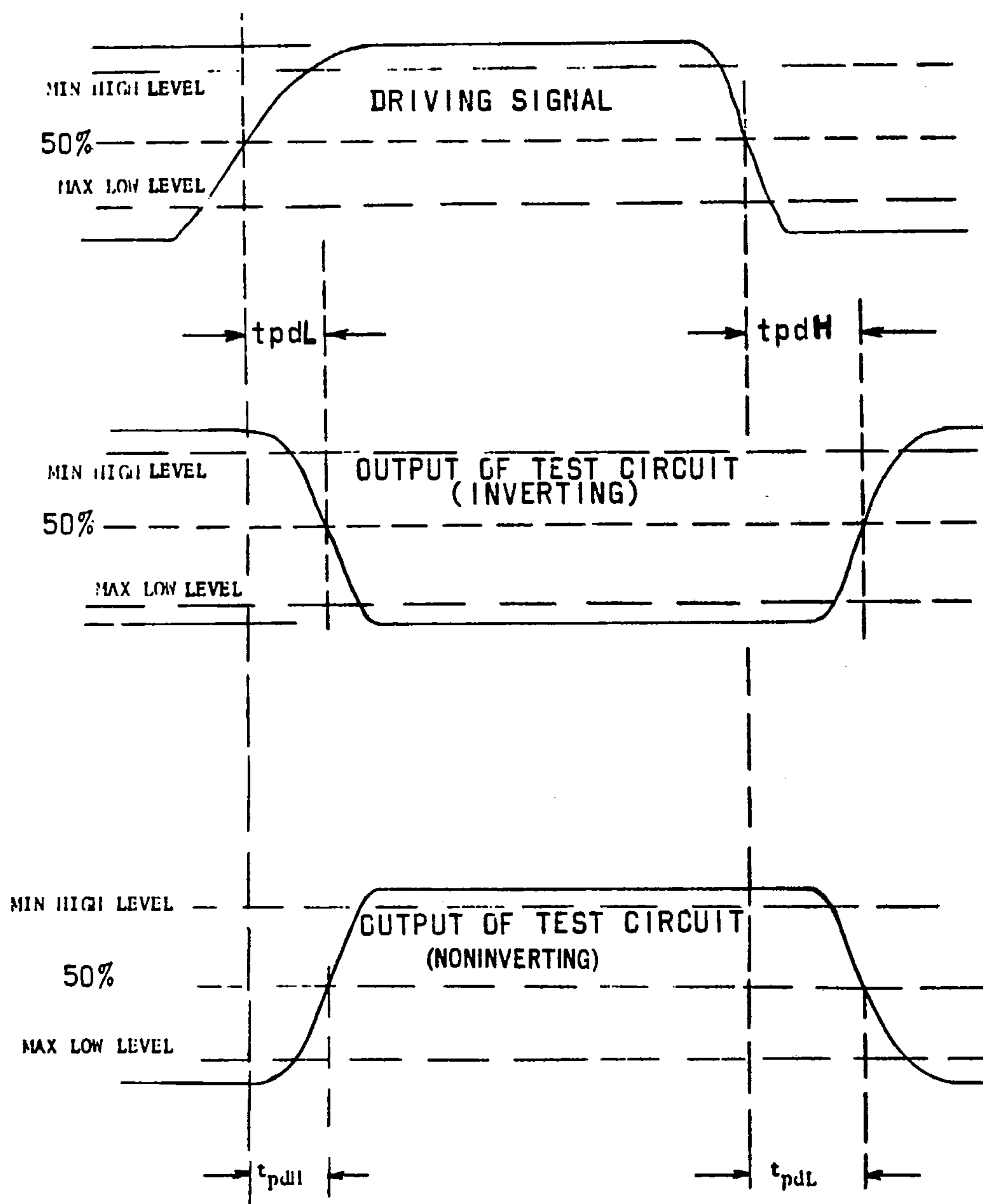

FIGURE 3003-2. Propagation delay.

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METHOD 3004

DELAY AND TRANSITION TIME MEASUREMENTS

1. PURPOSE. This method establishes the means for measuring the delay and output transitions times of logic gating circuits.

1.1 Definitions. The following definitions shall apply for the purpose of this method.

1.1.1 Rise time (t_r). The transition time of the output from 10% to 90% or 10% to a specified value of output voltage with the specified output changing from the defined low level to the defined high level.

1.1.2 Fall time (t_f). The transition time of the output from 90% to 10% or 90% to a specified value of output voltage with the specified output changing from the defined high level to the defined low level.

1.1.3 Transition delay time (t_{dLH}). The transition delay time measured with the output changing from 10% of the defined low level to the defined high level with respect to a 10% change in the corresponding input transition.

1.1.4 Transition delay time (t_{dHL}). The transition delay time measured with the output changing from 10% of the defined high level to the defined low level with respect to a 10% change in the corresponding input transition.

2. APPARATUS. Equipment capable of measuring the elapsed time between:

(a) The 10% to 90% or 10% to a specified voltage on the rise transition and the 90% to 10% or 90% to a specified voltage on the fall transition of the test circuit output shall be provided.

(b) The input signal and output signal at any voltage point between transition from the low level and the high level and from transition from the high level to the low level.

Accuracy of this equipment shall be defined in the applicable procurement document. It is desirable for this equipment to have data logging capability so that circuit dynamic performance distribution can be monitored.

3. PROCEDURE. The test circuit shall be loaded according to method 3002 of this standard. The driving signal to the test circuit shall be provided according to method 3001 of this standard.

3.1 Measurement of t_r and t_f. The rise transition time (t_r) at the output of the test circuit shall be measured from the 10% points to the 90% points or from the 10% points to a specified voltage point. Fall transition time (t_f) at the outputs of the test circuit shall be measured from the 90% points to the 10% points or from the 90% points to a specified voltage point. These measurements shall be made at the test circuit terminals. Figure 3004-1 shows typical transition readings.

3.2 Measurements of t_{dHL} and t_{dLH}. t_{dHL} shall be measured from the 10% point on the driving signal to the 90% point on the test circuit output signal for inverting logic. For noninverting logic, t_{dHL} shall be measured from the 90% point on the driving signal to the 90% point on the test circuit output signal. t_{dLH} shall be measured from the 90% point on the driving signal to the 10% point on the test circuit output signal for inverting logic. For noninverting logic, t_{dLH} shall be measured from the 10% point on the driving signal to the 10% point on the test circuit output signal. These delays shall be measured at the input and output terminal of the device under test. The values and tolerances on these delays shall be defined in the applicable procurement document. Figure 3004-1 shows typical delay readings.

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METHOD 3004 - Continued

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) t_r and tolerance.
(b) t_f and tolerance.
(c) Transition time measurement points if other than 10% or 90%.
(d) t_{dLH} and t_{dHL} limits.
(e) Parameters of the driving signal.
(f) Conditioning voltages.
(g) Load condition.
(h) Accuracy of measuring equipment.

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METHOD 3004 - Continued

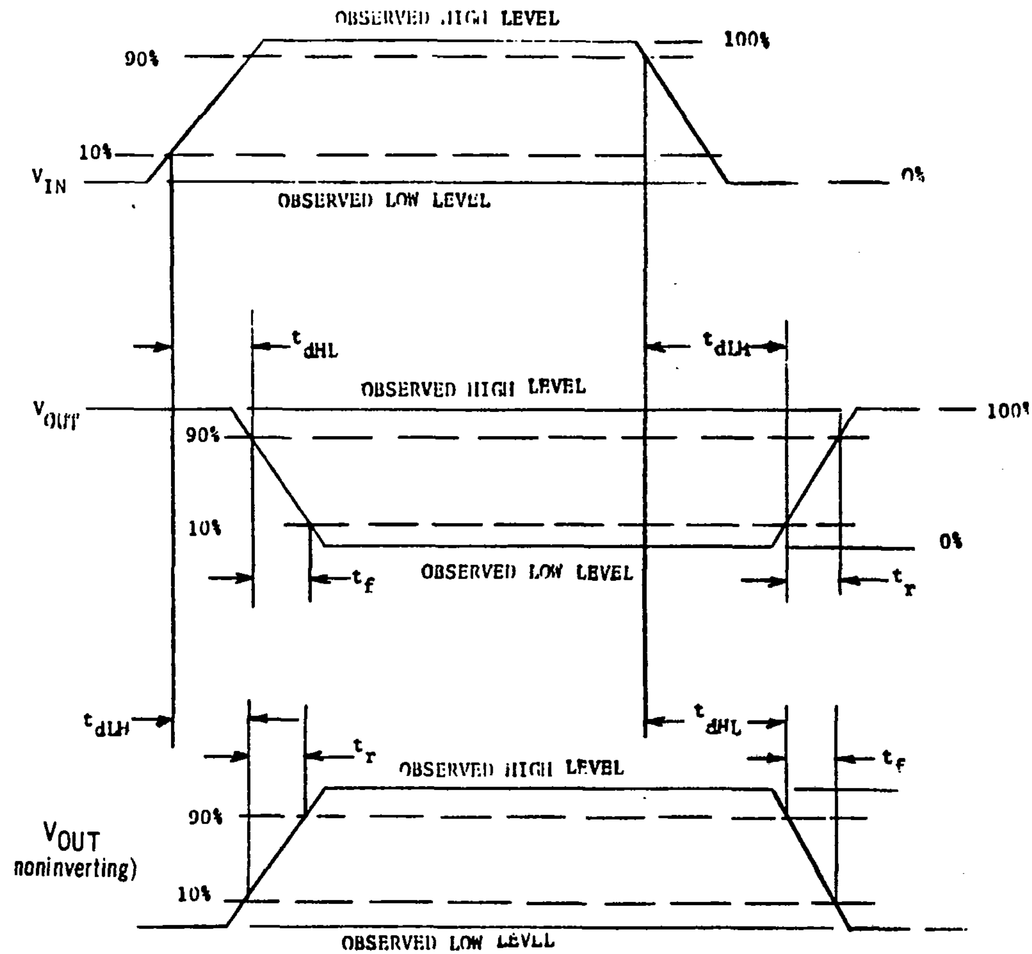
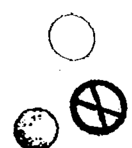


FIGURE 3004-1. Delay and transition time measurements on waveforms.



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METHOD 3005

POWER SUPPLY CURRENT

1. PURPOSE. This method establishes the means for measuring power supply currents (Icc) of logic gating circuits, such as TTL, RTL, ECTL, and DTL.

2. APPARATUS. Equipment capable of applying prescribed voltage to the test circuit power supply terminals and measuring the resultant currents flowing in these terminals shall be provided. This equipment shall also be capable of applying normal input levels to the test circuit and maintaining the device under test at any temperature between -55°C and +125°C.

3. PROCEDURE.

3.1 I_{ccH}. The test circuit shall be stabilized to the test temperature (T_A or T_J) specified in the applicable procurement document. Inputs of the device under test shall be conditioned in such a way as to provide an up level at the output, the worst case supply voltage(s) shall be applied and the resultant current flow in the supply terminals measured.

3.2 I_{ccL}. The test circuit shall be stabilized to the test temperature (T_A or T_J) specified in the applicable procurement document. Inputs of the device under test shall be conditioned in such a way as to provide a down level at the output, the worst case supply voltage(s) shall be applied and the resultant current flow in the supply terminals measured.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Test temperature (T_A or T_J).
(b) Power supply voltages.
(c) I_{ccH} and I_{ccL} limits.
(d) Conditioning of inputs.

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METHOD 3006

HIGH LEVEL OUTPUT VOLTAGE

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document in regard to high level output drive, which may be specified as a minimum value $V_{OH\ min}$ or as a maximum $V_{OH\ max}$. This method applies to TTL, DTL, RTL, and ECTL logic gating circuits.

2. APPARATUS. An instrument will be provided that has the capability of forcing current from the output terminal of the test circuit and measuring the resultant output voltage. Magnitude and tolerance of this current shall be defined in the applicable procurement document. In addition, the test instrument shall be capable of applying worst case power supply voltages, worst case levels to all inputs, and maintaining the test circuit at any temperature between -55°C and +125°C.

3. PROCEDURE. The circuit under test shall be stabilized to the test temperature (T_A or T_J) specified in the applicable procurement document. Worst case power supply voltages and worst case input levels including guaranteed noise margins shall then be applied to the test circuit to provide an up level output. For an inverting gate, each input in turn must be set at the maximum low level with all other inputs at the minimum high level. Current equal to the circuit worst case high level fan out shall be forced from the test circuit output terminal and the resultant output voltage measured.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Test temperature (T_A or T_J).
(b) Current to be forced from output terminal.
(c) Power supply voltage.
(d) Input levels.
(e) $V_{OH\ min}$ or $V_{OH\ max}$ limits.

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METHOD 3007

LOW LEVEL OUTPUT VOLTAGE

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document with regard to low level output drive which is specified as a maximum value ($V_{OL\ max}$) or a minimum value ($V_{OL\ min}$). This method applies to TTL, DTL, ECTL, and RTL logic gating circuits.

2. APPARATUS. An instrument shall be provided that has the capability of forcing current into the output terminal for TTL and DTL and forcing current from the output for RTL and ECTL of the test circuit and measuring the resultant output voltage. Magnitude and tolerance of this current shall be defined in the applicable procurement document. In addition, the test instrument shall be capable of applying worst case power supply voltages, worst case levels to all inputs, and maintaining the test circuit at any temperature between -55°C and +125°C.

3. PROCEDURE. The circuit under test shall be stabilized to the test temperature (T_A or T_J) specified in the applicable procurement document. Worst case power supply voltages and worst case input levels including guaranteed noise margins shall then be applied to the test circuit to provide a low level output. Current equal to the circuit worst case low level fan out shall be forced into the test circuit output terminal and the resultant output voltage measured.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Test temperature (T_A or T_J).
(b) Current to be forced into the output terminal for TTL and DTL and from the output terminal for RTL and ECTL equal to the worst case low level fan out.
(c) Power supply voltages.
(d) Input levels and noise margins.
(e) $V_{OL\ max}$ or $V_{OL\ min}$ limits.

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METHOD 3008

BREAKDOWN VOLTAGE, INPUT OR OUTPUT

1. PURPOSE. This method establishes the means for assuring device performance to the limits specified in the applicable procurement document in regard to input and output breakdown voltage symbolized as (BV_{IN}) and (BV_{OUT}), respectively.

2. APPARATUS. An instrument shall be provided that has the capability of forcing a specified voltage at the input or output terminal of the test circuit and measuring the resultant current flowing in that terminal. The test instrument shall also have the capability of applying voltage levels to all other terminals and maintaining the test circuit at the specified temperature. Care should be taken to assure that the test equipment does not inadvertently apply voltage to the device under test that will exceed the maximum rating of each terminal or that the current from the test equipment is sufficiently limited so that the device is not damaged.

3. PROCEDURE. The device under test shall be stabilized to the test temperature (T_A or T_J) specified in the applicable procurement document. Except for the test terminal, all other terminals shall be conditioned according to the applicable procurement document. A prescribed voltage shall be applied to the designated input or output and the resultant current shall be measured. When testing for input or output breakdown, all inputs or outputs shall be tested individually.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Test temperature (T_A or T_J).
(b) BV_{IN} and BV_{OUT}.
(c) Conditioning voltages for all other terminals.
(d) Maximum breakdown current limits.

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METHOD 3009

INPUT CURRENT, LOW LEVEL

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document in regard to low level input load which may be specified as a minimum value ($I_{IL\ MIN}$) or as a maximum value ($I_{IL\ MAX}$).

2. APPARATUS. An instrument shall be provided that has the capability of applying the worst case (most positive) down voltage to the input terminal of the test circuit, (and worst case levels on the other inputs) and measuring the resultant current flowing in the input terminal. Magnitude and tolerances of these voltages shall be defined in the applicable procurement document. In addition, the test instrument shall be capable of applying worst case power supply voltages and maintaining the test circuit at the specified temperature.

3. PROCEDURE. The circuit under test shall be stabilized to the test temperature (T_A or T_J) specified in the applicable procurement document. Worst case power supply voltages and worst case input voltages shall then be applied to the test circuit and the resultant current flowing in the input terminal shall be measured. All inputs shall be tested individually.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Test temperature (T_A or T_J).
(b) Power supply voltages.
(c) Input voltages.
(d) Worst case voltages at other input terminals.
(e) $I_{IL\ MAX}$ or $I_{IL\ MIN}$.

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METHOD 3010

INPUT CURRENT, HIGH LEVEL

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document in regard to high level input load which may be specified as a maximum value ($I_{IH\ MAX}$) or a minimum value ($I_{IH\ MIN}$).

2. APPARATUS. An instrument shall be provided that has the capability of applying the worst case (most negative) up voltage to the input terminal of the test circuit, and worst case levels at the other inputs, and measuring the resultant current flowing in the input terminal. Magnitude and tolerance of these voltages shall be defined in the applicable procurement document. In addition, the test instrument shall be capable of applying worst case power supply voltages and maintaining the test circuit at the specified temperature.

3. PROCEDURE. The circuit under test shall be stabilized to the test temperature (T_A or T_J) specified in the applicable procurement document. Worst case power supply voltages and worst case input voltages shall then be applied to the test circuit and the resultant current flowing in the input terminal shall be measured. All inputs shall be tested individually.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Test temperature (T_A or T_J).
(b) Power supply voltages.
(c) Input voltage.
(d) Worst case input voltages at other input terminals.
(e) $I_{IH\ MAX}$.

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METHOD 3011

OUTPUT SHORT CIRCUIT CURRENT

1. PURPOSE. This method establishes the means for assuring circuit performance to the limits specified in the applicable procurement document in regard to output short circuit current (I_{OS}). This method applies to TTL, DTL, ECTL, and RTL logic gating circuits.

2. APPARATUS. An instrument will be provided that has the capability of forcing a voltage of 0 volts at the output terminal of the device under test and measuring the resultant current flowing from that terminal. The test instrument will also have the capability of applying voltage levels to all other terminals and maintaining the test circuit at the specified temperature.

3. PROCEDURE. The device under test shall be pre-heated or cooled, until stabilized to the test temperature (T_A or T_J) specified in the applicable procurement document. Inputs of the device under test shall be conditioned in such a way as to provide a high level at the output. Worst case power supply voltages shall be applied. The output terminal shall be forced to the 0 volt potential and the resultant current flow measured. Care should be taken to assure that only one circuit per package is tested for the parameter at the same time.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Test temperature (T_A or T_J).
(b) Input conditioning voltages.
(c) Power supply voltages.
(d) $I_{OS\ MAX}$ and $I_{OS\ MIN}$ limits.

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METHOD 3012

TERMINAL CAPACITANCE

1. PURPOSE. This method established the means for assuring circuit performance to the limits specified in the applicable procurement document in regard to terminal capacitance. This method applies to all logic gating circuits.

2. APPARATUS. An instrument will be provided that has the capability of applying a 1 MHz controllable amplitude signal superimposed on a variable plus or minus DC voltage. The instrument will also have the capability of measuring the capacitance of this terminal to within the limits and tolerance specified in the applicable procurement document.

3. PROCEDURE. This test may be performed at room temperature. The capacitance measuring bridge shall be connected between the input or output terminal and the ground terminal of the test circuit. The bridge shall be adjusted for a signal of 1 MHz, 50 MV in amplitude riding a bias level specified in the applicable procurement document. With no device in the test socket the bridge shall then be zeroed. For capacitance values below 20 pf, the device shall be connected directly to the bridge with leads as short as possible to avoid the effects of lead inductance. After inserting the device under test and applying the specified bias conditions, the terminal capacitance shall be measured and compared to the limits listed in the applicable procurement document.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Circuit bias conditions.
(b) Bias level at which measurements are to be made.
(c) Maximum capacitance limits.

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METHOD 3013

NOISE MARGIN MEASUREMENTS FOR MICROELECTRONIC LOGIC GATING CIRCUITS

1. PURPOSE. This method establishes the means for measuring the DC (steady state) and AC (transient) noise margin of microelectronic logic gating circuits or to determine compliance with specified noise margin requirements in the applicable procurement document. It is also intended to provide assurance of interchangeability of devices and to eliminate misunderstanding between manufacturers and users on noise margin test procedures and results. The standardization of particular combinations of test parameters (e.g., pulse width, pulse amplitude, etc.) does not preclude the characterization of devices under test with other variations in these parameters. However, such variations shall, where applicable, be provided as additional conditions of test and shall not serve as a substitute for the requirements established herein.

1.1 Definitions. The following definitions shall apply for the purposes of this test method:

(a) Noise margin. Noise margin is defined as the voltage amplitude of extraneous signal which can be algebraically added to the noise-free worst case "input" level before the output voltage deviates from the allowable logic voltage levels. The term "input" (in quotation marks) is used here to refer to logic input terminals or ground reference terminals.

(b) DC noise margin. DC noise margin is defined as the DC voltage amplitude which can be algebraically added to the noise-free worst case "input" level before the output exceeds the allowable logic voltage levels.

(c) AC noise margin. AC noise margin is defined as the transient or pulse voltage amplitude which can be algebraically added to the noise-free worst case "input" level before the output voltage exceeds the allowable logic voltage levels.

1.2 Symbols. The following symbols shall apply for the purposes of this test method and shall be used in accordance with the definitions provided (see 1.2.1, 1.2.2, and 1.2.3) and depicted in figures 3013-1, 3013-2, and 3013-3.

1.2.1 Logic levels.

$V_{IL\ max}$: The maximum allowed input "low" level in a logic system.

$V_{IL\ min}$: The minimum allowed input "low" level in a logic system.

$V_{IH\ max}$: The maximum allowed input "high" level in a logic system.

$V_{IH\ min}$: The minimum allowed input "high" level in a logic system.

$V_{OL\ max}$: The maximum output "low" level specified for a logic gating circuit. $V_{OL\ max}$ is also the noise-free worst case input "zero" level.

$$V_{OL\ max} \leq V_{IL\ max}$$

$V_{OH\ min}$: The minimum output "high" level specified for a logic gating circuit. $V_{OH\ min}$ is also the noise-free worst case input "high" level.

$$V_{OH\ min} \geq V_{IH\ min}$$

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METHOD 3013 - Continued

1.2.2 Noise margin levels.

V_{NL}: The "low" level noise margin, or input voltage amplitude which can be algebraically added to $V_{OL\ max}$ before the output level exceeds the allowed logic level.

V_{NH}: The "high" level noise margin, or input voltage amplitude which can be algebraically added to $V_{OH\ min}$ before the output level exceeds the allowed logic level.

V_{NG+}: The positive voltage which can be algebraically added to the ground level before the output exceeds the allowed logic level determined by worst case logic input levels.

V_{NG-}: The negative voltage which can be algebraically added to the ground level before the output exceeds the allowed logic level determined by worst case logic input levels.

V_{NP+}: The positive voltage which can be algebraically added to the noise-free worst case upper power supply voltage before the output exceeds the allowed logic level determined by worst case logic input levels.

V_{NP-}: The negative voltage which can be algebraically added to the noise-free worst case lower power supply voltage before the output exceeds the allowed logic level determined by worst case logic input levels.

1.2.3 Noise pulse widths.

PW_L: The "low" level noise pulse width, measured at the $V_{IL\ max}$ level.

PW_H: The "high" level noise pulse width, measured at the $V_{IH\ min}$ level.

PW_{G+}: The positive ground noise pulse width, measured at the 50% amplitude level.

PW_{G-}: The negative ground noise pulse width, measured at the 50% amplitude level.

PW_{p+}: The positive power supply noise pulse width, measured at the 50% amplitude level.

PW_{p-}: The negative power supply noise pulse width, measured at the 50% amplitude level.

2.2 APPARATUS. The apparatus used for noise margin measurements shall include a suitable source generator (see 2.1), load (see 2.2), and voltage detection devices for determining logic state.

2.1 Source generator. The source generator for this test shall be capable of supplying the required AC and DC noise inputs. In the case of pulsed inputs the rise and fall times of the injected noise pulse shall each be maintained to less than 20% of the pulse width measured at the 50% amplitude level. For the purpose of this criteria, the rise and fall times shall be defined as the transition times between the 10% and 90% amplitude levels. The pulse repetition rate shall be sufficiently low that the element under test is at steady-state conditions prior to the application of the noise pulse. For the purpose of this criteria, doubling the repetition rate or duty cycle shall not affect the outcome of the measurement.

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METHOD 3013 - Continued

2.2 Load. The load for this test shall simulate the circuit parameters of the normal load which would be applied in application of the device under worst-case conditions. The load shall automatically change its electrical parameters as the device under test changes logic state if this is the normal situation for the particular device load. The load shall be paralleled by a high impedance voltage detection device.

3. PROCEDURE. The device shall be connected for operation using a source generator and load as specified (see 2), and measurements shall be made of V_{NL}, V_{NH}, V_{NG}, and V_{NP} following the procedures for both AC noise margin and DC noise margin (see 3.2 through 3.3.5).

3.1 General considerations.

3.1.1 Non-propagation of injected noise. As defined in 1.1, noise margin is the amplitude of extraneous signal which may be added to a noise-free worst case "input" level before the output breaks the allowable logic levels. This definition of noise margin allows the measurement of both DC and AC noise immunity on logic inputs or power supply lines or ground reference lines by detection of either a maximum "low" level or a minimum "high" level at the output terminal. Since the output level never exceeds the allowable logic level under conditions of injected noise, the noise is not considered to propagate through the element under test.

3.1.2 Superposition of simultaneously injected noise. Because the logic levels are restored after one stage, and because the noise margin measurement is performed with all "inactive" inputs at the worst case logic levels, the proper system logic levels are guaranteed in the presence of simultaneous disturbances separated by at least one stage.

3.1.3 Characterization of AC noise margin. Although the purpose of this standard test procedure is to insure interchangeability of elements by a single-point measurement of AC noise margin, the test procedure is well suited to the measurement of AC noise margin as a function of noise pulse width. In particular, for very wide pulse widths, the AC noise margin asymptotes to a value identically equal to the DC noise margin.

3.2 Test procedure for DC noise margin.

3.2.1 Worst case configuration. The measurement of DC noise margin using a particular logic input terminal should correspond to the worst case test configuration in the applicable procurement document. For example, the measurement of "low" level noise margin for a positive-logic inverting NAND gate should be performed under the same worst case test conditions as the DC measurement of $V_{OH\ min}$. If the worst case DC test conditions for $V_{OH\ min}$ are high power supply voltage, all unused logic inputs connected to $V_{OH\ min}$ and output current equal to zero, these conditions should be applied to the corresponding DC noise margin measurement.

3.2.2 "Low" level noise margin, V_{NL}. With all unused logic inputs connected to the worst case voltage, worst case power supply voltages applied, and worst case output loading, increase the voltage at the input under test until the output level equals $V_{IH\ min}$ for inverting elements, or $V_{IL\ max}$ for noninverting elements. The DC "low" level noise margin is the amplitude of the input voltage minus the noise-free worst case value, $V_{OL\ max}$.

3.2.3 "High" level noise margin, V_{NH}. With all unused inputs connected to the worst case voltage, worst case power supply voltages applied, and worst case output loading, decrease the voltage at the input under test until the output level equals $V_{IL\ max}$ for inverting elements, or $V_{IH\ min}$ for noninverting elements. The DC "high" level noise margin is the difference between the noise-free worst case input level, $V_{OH\ min}$, and the input voltage measured.

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METHOD 3013 - Continued

3.2.4 Ground noise margin, V_{NG+} or V_{NG-}. With all input, power supply and output terminals connected to the appropriate worst case conditions, increase (or decrease) the voltage applied to the ground terminal until the output level equals the appropriate logic level limit. The DC ground noise margin is the voltage measured at the ground terminal. Note that the worst case test conditions may be different for positive and negative ground noise tests. The DC source resistance of the injected ground line voltage should be negligibly small.

3.2.5 Power supply noise margin, V_{NP+} or V_{NP-}. With all input, power supply, and output terminals connected to the appropriate worst case conditions, increase(or decrease) the power supply voltage(s) until the output level equals the appropriate logic level limit. The power supply noise margin is the difference between the measured supply voltage(s) and the appropriate noise-free worst case supply voltage level(s). If more than one power supply is required, the noise margin of each supply should be measured separately.

3.3 Test procedure for AC noise margin.

3.3.1 AC noise margin test point. If, for any combination of noise pulse width or rise and fall times, the AC noise margin is less than the DC noise margin, the noise pulse amplitude, pulse width, and rise or fall time which produce the minimum noise margin shall be used as the conditions for test.

If the AC noise margin exceeds the DC noise margin for all combinations of noise pulse width or rise and fall time, the noise pulse width used as the condition for this test shall be that width at which the AC noise margin is equal to twice the DC noise margin. If the AC margin exceeds the DC margin by less than this factor of two, then the AC margin shall be defined as equal to the DC noise margin for all pulse widths.

3.3.2 "Low" level noise margin, V_{NL}. With all unused logic input, power supply, and output terminals connected to appropriate worst case conditions, a positive-going noise pulse shall be applied to the input under test. Pulse amplitude and width shall be in accordance with 3.3.1. Pulse width, PW_L, shall be measured at the level V_{IL} max.

3.3.3 "High" level noise margin, V_{NH}. With all unused logic input, power supply, and output terminals connected to appropriate worst case conditions, a negative-going noise pulse shall be applied to the input under test, in accordance with 3.3.1. Pulse width, PW_H, shall be measured at the level V_{IH} min.

3.3.4 Ground noise margin, V_{NG+} or V_{NG-}. With all input, power supply and output terminals connected to appropriate worst case conditions, a positive (or negative)-going pulse shall be applied to the ground terminal, in accordance with 3.3.1. Pulse width PW_{G+} (or PW_{G-}) shall be measured at the 50% amplitude level.

3.3.5 Power supply noise margin, V_{NP+} or V_{NP-}. With all input, power supply, and output terminals connected to appropriate worst case conditions, a positive (or negative)-going pulse shall be superimposed on the power supply terminal(s), in accordance with 3.3.1. Pulse width, PW_{P+} (or PW_{P-}) shall be measured at the 50% amplitude level.

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4. SUMMARY. The following details, when applicable, shall be specified in the applicable procurement document:

(a) V_{IL} max

(b) V_{IL} min

(c) V_{IH} min

(d) V_{IH} max

(e) V_{OL} max

(f) V_{OH} min

(g) V_{NL}

(h) V_{NH}

(i) V_{NG}

(j) V_{NP}

(k) Test temperature. Unless otherwise specified, noise margin measurements shall be made at the rated operating temperature extremes in addition to any other nominal test temperatures.

(l) Specific noise margin measurements and conditions which are to be performed.

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METHOD 3013 - Continued

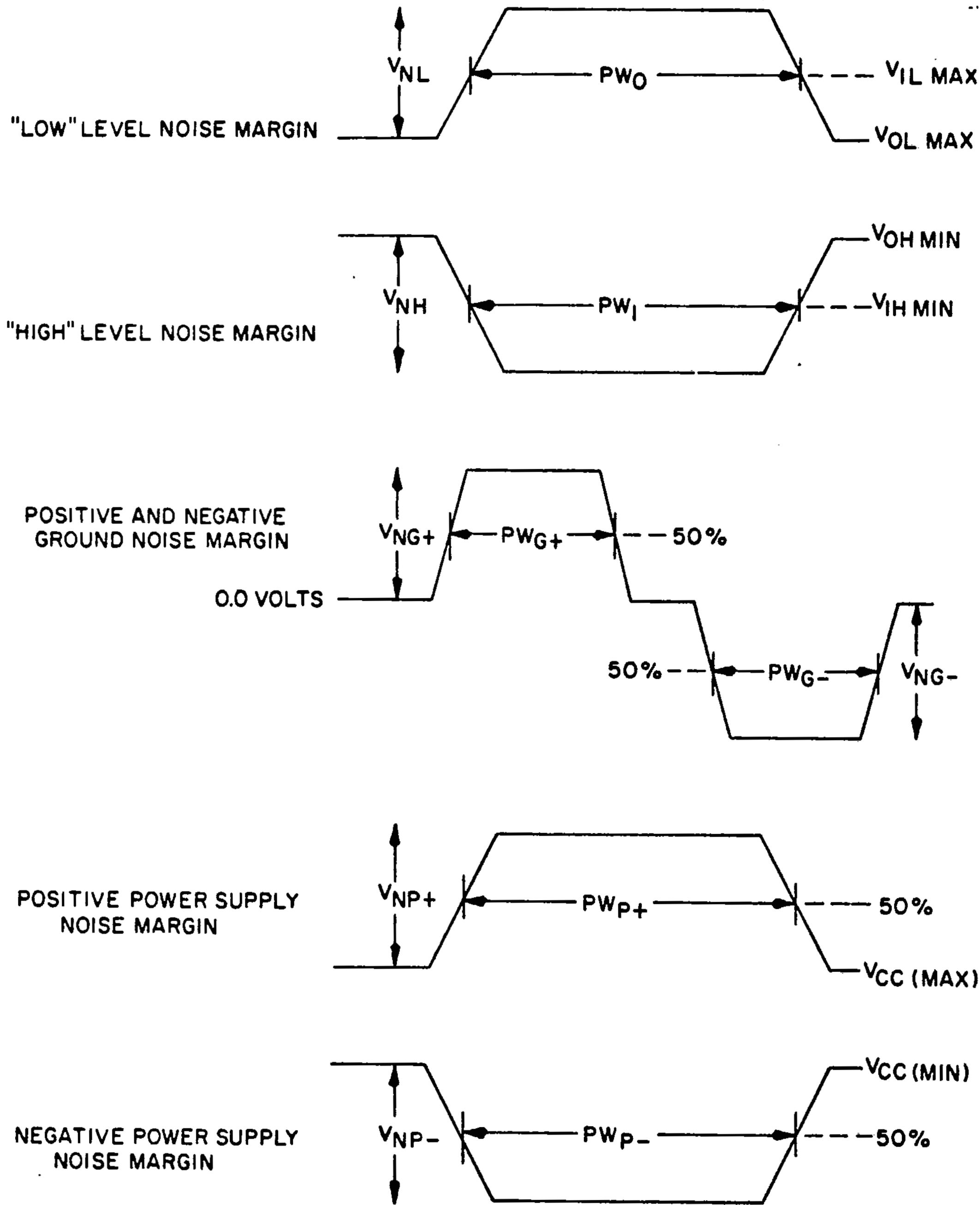

FIGURE 3013-1. Definitions of noise amplitude and pulse width.

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METHOD 3013 - Continued

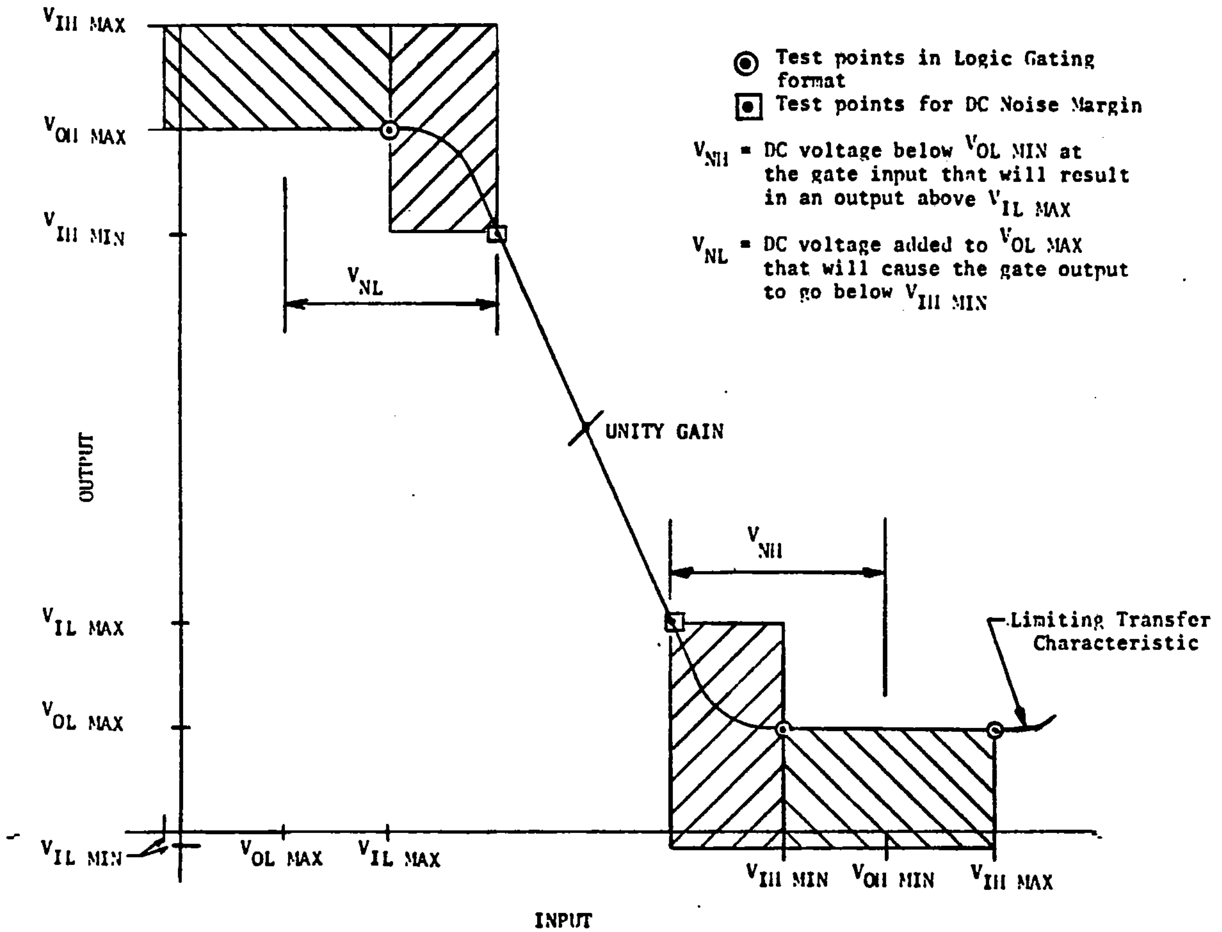

FIGURE 3013-2. Inverting logic gate transfer characteristic defining test points.

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METHOD 3013 - Continued

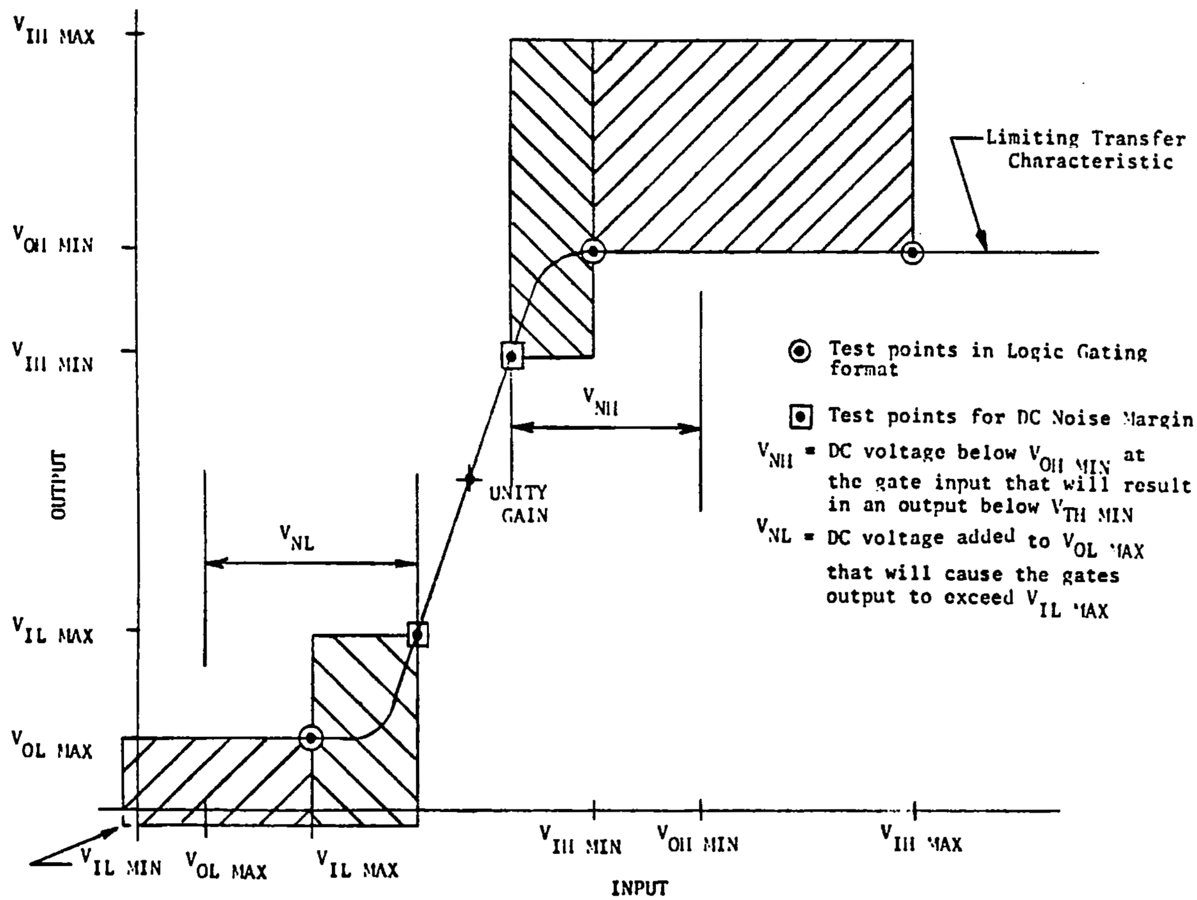

FIGURE 3013-3. Noninverting logic gate transfer characteristic defining test points.

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METHOD 4001

INPUT OFFSET VOLTAGE AND CURRENT AND BIAS CURRENT

1. PURPOSE. This method establishes the means for measuring input bias current and the offset in voltage and current at the input of a linear amplifier with differential inputs. Offset voltage may also be pertinent in some single input amplifiers. Input bias current will also be measured in this procedure.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Input offset voltage (V_{io}). That DC voltage which must be applied between the input terminals through two equal resistances to force the quiescent DC output to zero or other specified level V_{qo}.

1.1.2 Input offset voltage drift (DVio). Input offset voltage drift is the ratio of the change of input offset voltage to the change of circuit temperature.

$$DV_{io} = \frac{\Delta V_{io}}{\Delta T}$$

1.1.3 Input offset current (I_{io}). The input offset current is the difference between the currents entering into the input terminals of a differential input amplifier required to force the output voltage to zero or other specified level (V_{qo}).

1.1.4 Input offset current drift (DI_{io}). The input offset current drift is the ratio of the change of input offset current to the change of circuit temperature.

$$DI_{io} = \frac{\Delta I_{io}}{\Delta T}$$

1.1.5 Input bias current (I_{in}). The input bias current is one-half the sum of the separate currents entering into the two input terminals of a balanced amplifier.

2. APPARATUS. The apparatus shall consist of a suitable DC voltmeter and precision resistors. In the case of single input noninverting amplifiers and inverting amplifier will also be required.

2.1 DC voltmeter. The DC voltmeter shall have an input impedance sufficiently high as not to load the circuit under test. Accuracy shall be adequate so that it will have less than 10 percent effect on the tolerance specified for the circuit tested. For example, if a reading should be 0 ± 0.1V to be acceptable for the circuit tested the voltmeter shall be accurate to within ± 0.01V.

2.2 Resistor networks. Resistor networks used in the test circuit shall be within 1 percent or better of the specified values over the required temperature range.

2.3 Stabilization networks. Stabilization networks shall be appropriate to stabilize the circuit to prevent oscillation with 100% feedback (i.e., worst case conditions).

2.4 Inverting amplifier. A stabilized inverting amplifier shall have a DC gain of one accurate to 1 percent or better and offset of less than 10 MV, and shall be frequency compensated so that it presents the dominant pole in the overall test loop response. The input impedance of the inverting amplifier shall be at least 10 times Z_{out} of the circuit under test.

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METHOD 4001 - Continued

3. PROCEDURE. There are three test figures shown of which only one will be appropriate for a particular circuit type. R_2 shall be no larger than the nominal input impedance nor less than a value which will load the amplifier (10 x Z_{OUT}). Let $\frac{R_2}{R_1}$ = 100 or 0.1 x (open loop gain), whichever is smaller. Recommended stabilization and power supply decoupling circuitry shall be added. Let R_3 be a convenient value no larger than the nominal input impedance. The choice of values is based on keeping the inherent test error within 10% considering the assumptions normally applied in the use of operational amplifiers (e.g., infinite gain and input impedance with zero output impedance). The complete equation for an amplifier configuration as shown in figure 4001-4 is:

$$E_o - V_{qo} = \left[\left(\frac{R2}{R1}\right)(V_i - V_{qi}) + \left(\frac{R2}{Rin}\right)\left(1 + \frac{R1}{R2} + \frac{R1}{Rin}\right)V_{io}\right]\left[\frac{1}{1 + \frac{1}{A_v}\left(1 + \frac{R_2}{R_i} + \frac{R_2}{R_{in}}\right)}\right]$$

For measurements in this method, V_I as shown in figure 4001-4 equals zero. Where measurements are desired with inherent errors of less than 10%, appropriate adjustments in the component values may be made.

3.1 Input offset voltage.

3.1.1 Differential input amplifier. The test setup is shown in figure 4001-1. Input offset voltage $V_{io} = \frac{R_1}{R_2}(E_o - V_{qo})$. Switches S_1 and S_2 are closed for this test.

3.1.2 Single ended inverting amplifier. The test figure is shown in figure 4001-2. $V_{io} = \frac{R_1}{R_2}(E_o - V_{qo})$. Switch S is closed for this test.

3.1.3 Single ended noninverting amplifier. The test figure is shown in figure 4001-3. $V_{io} = \frac{R_1}{R_2}(E_o - V_{qo})$. Switch S is closed for this test.

3.2 Input offset current. This has a meaning for differential input amplifiers only.

3.2.1 Differential input amplifier. The test figure is shown in figure 4001-1. Measure E_{o1} with S_1 and S_2 closed, measure E_{o2} with S_1 and S_2 open.

$$I_{io} = \frac{R_1}{R_2}\left(\frac{E_{o1} - E_{o2}}{R_3}\right)$$

3.3 Input bias current.

3.3.1 Differential input amplifier. The test figure is shown in figure 4001-1. Measure E_{o1} with S_1 open and S_2 closed, measure E_{o2} with S_1 closed and S_2 open.

$$I_{in} = \frac{R_1}{R_2}\left(\frac{E_{o1} - E_{o2}}{2R_3}\right)$$

3.3.2 Single ended inverting amplifier. The test figure is shown in figure 4001-3. Measure E_{o1} with S closed, measure E_{o2} with S open.

$$I_{in} = \frac{R_1}{R_2}\left(\frac{E_{o2} - E_{o1}}{R_3}\right)$$

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METHOD 4001 - Continued

3.3.3 Single ended noninverting amplifier. The test figure is shown in figure 4001-3. Measure E_{o1} with S closed. Measure E_{o2} with S open.

$$I_{in} = \frac{R_1}{R_2}\left(\frac{E_{o2} - E_{o1}}{R_3}\right)$$

3.4 Input offset voltage drift. Measurement of V_{io1} is made at temperature T_1 per section 3.1 and a second measurement at T_2 of V_{io2} is made at the second temperature.

$$DV_{io} = \frac{V_{io2} - V_{io1}}{T_2 - T_1}$$

3.5 Input offset current drift. Measurement of I_{io1} is made at temperature T_1 and I_{io2} at temperature T_2 per section 3.2.

$$DI_{io} = \frac{I_{io2} - I_{io1}}{T_2 - T_1}$$

4. SUMMARY. The following details shall be specified in the applicable procurement document for specified values of R_1, R_2, and R_3.

(a) V_{io} maximum.
(b) DV_{io} maximum at specified temperature(s).
(c) I_{io} maximum when applicable.
(d) DI_{io} maximum, when applicable, at specified temperature(s).
(e) I_{in} maximum at specified temperature(s).
(f) V_{qi} and V_{qo}, when applicable, at specified temperature(s).
(g) Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperature and at 25°C ambient.

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METHOD 4001 - Continued

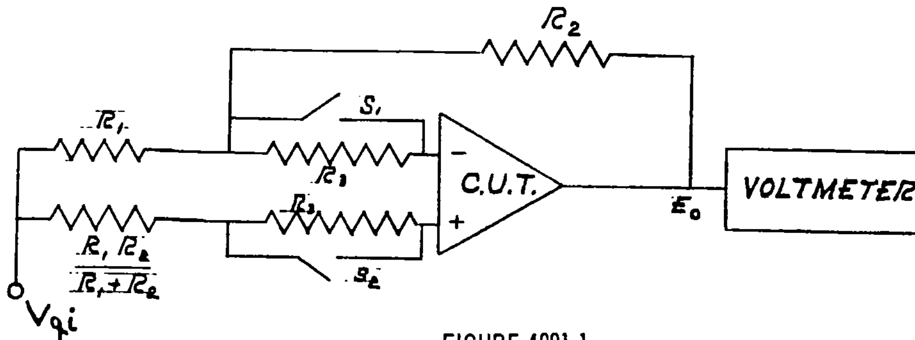

FIGURE 4001-1

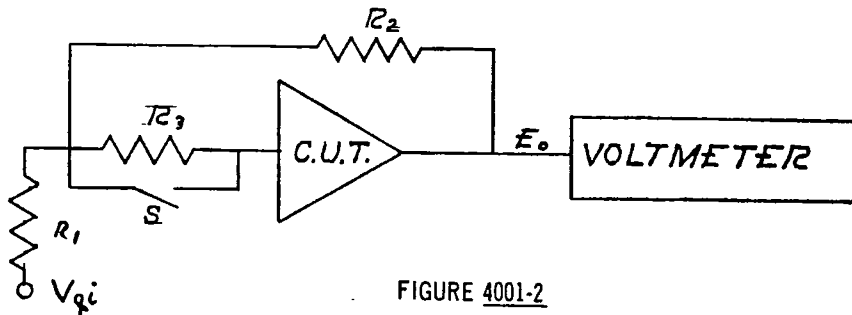

FIGURE 4001-2

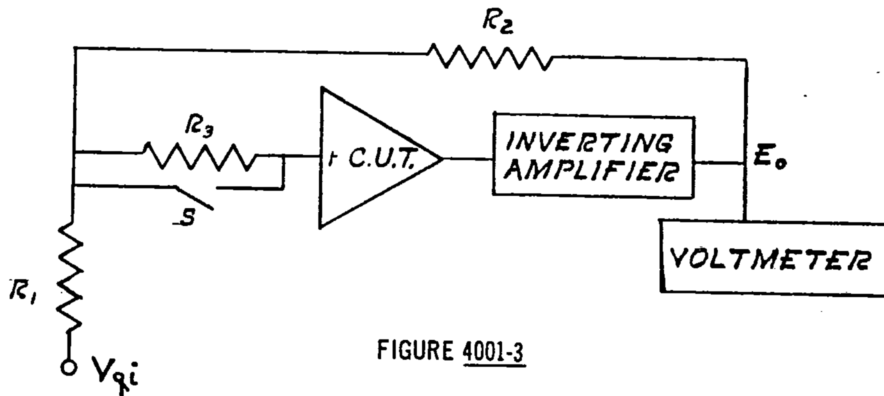

FIGURE 4001-3

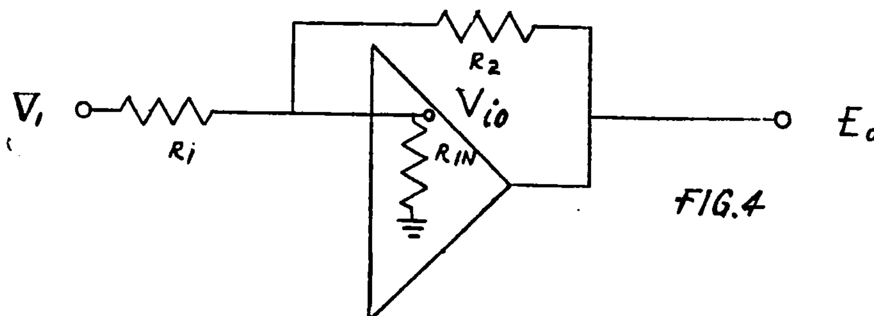

FIGURE 4001-4

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METHOD 4002

PHASE MARGIN AND SLEW RATE MEASUREMENTS

1. PURPOSE. This method establishes the means for measuring the stability and slew rate of a linear amplifier intended to be used with feedback.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Phase margin. The phase margin is 180° minus the absolute value of the phase shift measured around the loop at that frequency at which the magnitude of the loop gain is unity. The loop is the series path of the device under test and the feedback network which is opened at the inverting terminal. The inverting terminal is loaded down to simulate the load normally presented by the feedback network. Good practice dictates that the phase margin should be at least 45°.

1.1.2 Peaking. If a closed loop gain versus frequency plot is made, peaking is the amount by which the gain may increase over its nominal value just before it falls off. 3 db of peaking will result from a phase margin of 45°. Thus it is desirable to keep the peaking less than 3 db.

1.1.3 Slew rate. Slew rate is the time rate of change of the closed-loop amplifier output voltage under large signal conditions (i.e., the maximum AC input voltage for which the amplifier performance remains linear). Stabilization networks will affect the slew rate and therefore these must be included in the measurement.

2. APPARATUS. The apparatus will consist of a video sweep generator, pulse generator, oscilloscope, precision resistors, and stabilization networks.

2.1 Sweep generator. The sweep generator must cover the frequency range of the amplifier under test. It shall have an adjustable output level of at least 1 volt and flat to ± 0.2 db over the sweep range.

2.2 Pulse generator. The pulse generator shall have an output pulse with rise and fall times sufficiently short so as to not degrade the slew rate measurement.

2.3 Oscilloscope. The oscilloscope shall have a frequency response wider than the circuit under test and shall be compatible with both the sweep generator and pulse generator for synchronization.

2.4 Resistor networks. The resistors shall be within 1 percent or better of the specified values.

2.5 Stabilization networks. Stabilization networks shall be appropriate to stabilize the circuit for adequate phase margin with feedback.

3. PROCEDURE. The test figures show the connections for the various test conditions. Recommended stabilization networks should be added to compensate for the degree of feedback in the test. The circuit under test should have adequate power supply decoupling added. For differential output devices, the measurements described in 3.1 thru 3.2.1 below, as applicable, shall be repeated for the other output using the same test figure except that the cathode ray oscilloscope shall be connected to the other output.

3.1 Phase margin. The test shall be set up as in figure 4002-1 for a gain of 1 noninverting. This is the maximum feedback case. R_2 and R_1 shall be the same value and shall be low compared to the amplifier input impedance. Figure 4002-2 shows the amplitude of the envelope of the output E_0. The peaking shall be less than 3 db (1.414 times the flat band voltage) to indicate a 45° phase margin minimum. The circuit of figure 4002-3 shall be used for single ended inverting amplifiers (where no positive input terminal is brought out) or where the test is to be run at closed loop gains greater than 1. Closed loop gain = $\frac{R_2}{R_1}$. In the case of closed loop gains greater than one of the peaking shall be less than 3 db.

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METHOD 4002 - Continued

3.2 Pulsed slew rate. Figure 4002-4 is the test figure for this test. Values of R_2 and R_1 shall be the same values as those used in the phase margin test. Stabilization networks shall also be the same. The pulse amplitude V_1 shall be such that E_0 is the maximum large signal value for the amplifier. With the pulse V_1 having a rise and fall time much faster than the specified slew rate for the amplifier the rise and fall time for the amplifier shall be measured. These shall be within specified limits (see 4). The test shall be repeated for both polarities of V_1. This is the preferred technique for slew rate measurements.

3.2.1 Sinusoidal slew rate. This is an alternate procedure to the preferred procedure of 3.2. Apply a sinusoidal signal at the input of the circuit under test at the specified initial frequency and of sufficient amplitude to cause the circuit output voltage to swing to its maximum values. Maintaining the input signal level constant, increase the frequency from the specified initial frequency to the frequency where the output swing decreases 3 db. This frequency, converted to units of time, and the swing, give the measure of slew rate. Figure 4002-4 is the test figure for this test with the pulse generator replaced by a sinusoidal generator of appropriate frequency and output characteristics. Values of R_2 and R_1 and stabilization networks shall be the same as those used in the phase margin test.

4. SUMMARY. The following details shall be specified in the applicable procurement document for specified values of R_1, R_2, and V_1:

(a) Maximum peaking.
(b) Maximum rise time for E_0 positive pulses.
(c) Maximum fall time for E_0 positive pulses.
(d) Maximum rise time for E_0 negative pulses.
(e) Maximum fall time for E_0 negative pulses.
(f) Procedure for slew rate (see 3.2 and 3.2.1) and initial frequency, when applicable, for sinusoidal slew rate measurement (see 3.2.1).
(g) Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperatures and at 25°C ambient.

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METHOD 4002 - Continued

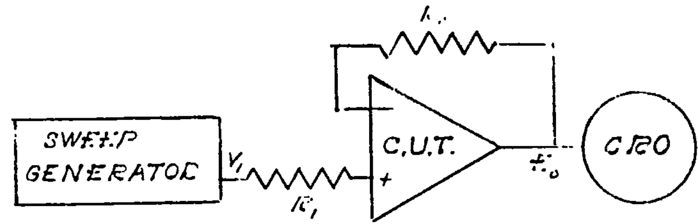

FIGURE 4002-1

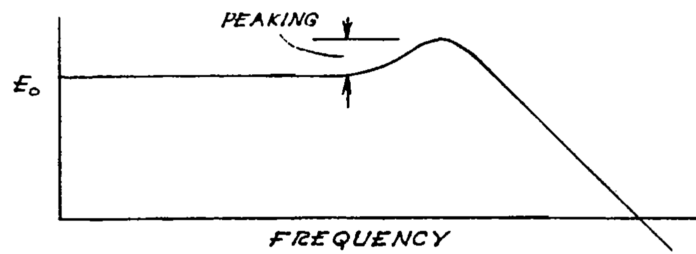

FIGURE 4002-2

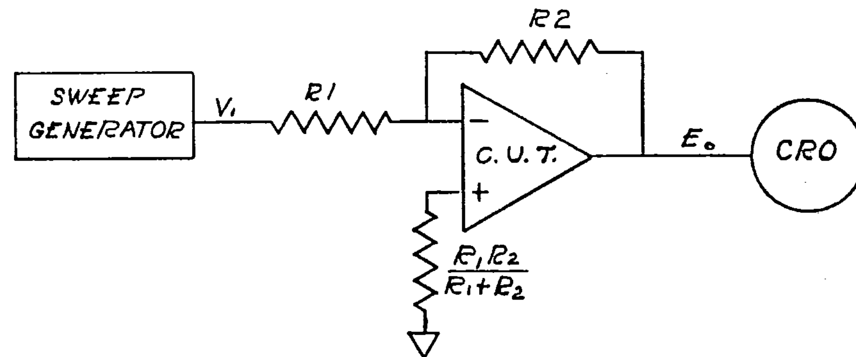

FIGURE 4002-3

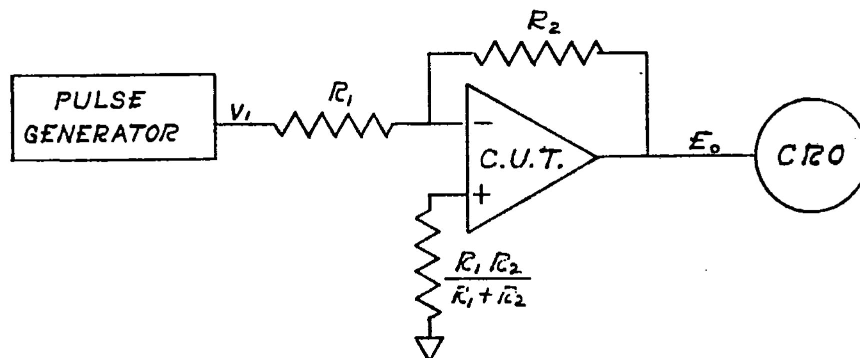

FIGURE 4002-4

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METHOD 4003

COMMON MODE INPUT VOLTAGE RANGE
COMMON MODE REJECTION RATIO
SUPPLY VOLTAGE REJECTION RATIO

1. PURPOSE. This method establishes the means for measuring common mode input voltage range, common mode rejection ratio, and supply voltage rejection ratio.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Common mode input voltage range (V_{cmi}). The common mode input voltage range is that range of common mode input voltages which if exceeded will cause the amplifier to distort or is that range of voltage which may be applied to the input terminals of the device without decreasing the common mode rejection ratio (CM_{rr}) by more than 6 db.

1.1.2 Common mode rejection ratio (CM_{rr}). The common mode rejection ratio is the ratio of the differential open loop gain, A_d, to the common mode voltage gain, A_c.

$$CM_{rr} = \frac{A_d}{A_c}$$

CM_{rr} is usually expressed in decibels:

$$CM_{rr} = 20 \text{ Log } \frac{A_d}{A_c}$$

1.1.3 Power supply rejection ratio (PS_{rr}). The power supply rejection ratio is the ratio of the change in input offset voltage ΔV_{io}, to the corresponding change in one power supply voltage with all remaining power supply voltage(s) held constant.

$$PS^{+}_{rr} = \frac{\Delta V_{io}}{\Delta V_{cc}} \qquad V_{bb} = \text{constant}$$

$$PS^{-}_{rr} = \frac{\Delta V_{io}}{\Delta V_{bb}} \qquad V_{cc} = \text{constant}$$

The power supply rejection ratio can also be expressed in terms of open loop gain, A_d, change in output voltage, ΔV_o, and corresponding change in power supply voltage, ΔV_{cc} or ΔV_{bb}.

$$PS_{rr} = \frac{\Delta V_o}{A_d \, \Delta V_{cc}}$$

2. APPARATUS. The apparatus shall consist of a suitable signal generator, AC voltmeter, power supply, low pass filter, capacitors, and precision resistors.

2.1 Signal generator. The signal generator shall be capable of supplying a sine wave output with less than 1 percent distortion when loaded with its characteristic impedance and adjusted for maximum output power. The distortion shall not become greater at lower output power settings. Distortion shall be checked at frequencies of interest for this test. Output impedance shall be less than 100 ohms. The output shall be AC coupled.

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METHOD 4003 - Continued

2.2 AC voltmeter. The AC voltmeter shall be calibrated in peak volts. Input impedance shall be sufficiently high so the loading of the circuit under test will be negligible. Accuracy in the range of frequencies of interest should be adequate so that it will have less than 10 percent effect on the tolerance specified for the circuit tested.

2.3 Power supply. The power supply shall be capable of supplying maximum required input power to the test circuit.

2.4 Low pass filter. This filter shall be capable of isolating signal frequencies introduced on the power input of the test circuit from the power supply. The purpose of this filter is to eliminate the possibility of driving the power supply used in the test set-up out of regulation. It should be specified in conjunction with the power supply to be used and the signal frequencies of interest, and shall be sufficient to limit the maximum total noise and ripple of the power supply and filter combination to 5% or less of the test signal level.

2.5 Capacitor. The capacitors shall have a tolerance of ±10 percent or better over the temperature range of interest. Leakage and equivalent inductance shall be negligible at the frequencies and temperatures of interest.

2.6 Resistor networks. Resistor networks are used in the test circuit. These shall have a tolerance of ± 1 percent or better over the required temperature range.

2.7 Stabilization networks. Stabilization networks shall be appropriate to stabilize the circuit to prevent oscillation with feedback.

3. PROCEDURE. There are two test figures shown. Figure 4003-1 shall be used for common mode input voltage range and common mode rejection ratio tests. Figure 4003-2 shall be used for supply voltage rejection ratio. R_1 shall be no larger than the nominal input impedance nor less than a value which will load the amplifier (100 x Z_{out}). Specified stabilization and power supply decoupling shall be added where applicable. R_2 shall be approximately equal to R_1 and C_2 approximately equal to C_1. $2\pi f \; R_1 C_1$ shall be at least $10A_d$ where A_d is the open loop gain and f is the frequency. Referring to the circuit in figure 4003-3 the transfer function is:

$$\frac{E_0}{E_1} = \frac{A_v}{1 + \frac{(A_v + 1)(R_s - jX_c)}{R_1}}$$

The error term, which indicates the degree of unbalance between the two inputs is:

$$\frac{(A_v + 1)(R_s - jX_c)}{R_1}$$

This error term shall be maintained below a value of 0.1.

3.1 Common mode input voltage range.

3.1.1 Differential input amplifier. This test shall be an implied measurement. The maximum common mode input voltage specified for the amplifier shall be used in making the common mode rejection ratio test of 3.2.

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METHOD 4003 - Continued

3.2 Common mode rejection ratio.

3.2.1 Differential input amplifier. The test setup shall be as shown in figure 4003-1. The signal frequency shall be as specified.

$$A_c = \frac{V_o}{V_i}$$

Where: A_c = Common mode voltage gain

V_o = Common mode output voltage (peak)

V_i = Common mode input voltage, maximum (peak)

and:

$$CM_{rr} = 20 \text{ Log } \frac{A_d}{A_c}$$

3.3 Power supply rejection ratio.

3.3.1 Differential input amplifier. This test setup shall be as shown in figure 4003-2. The power supply shall be adjusted for a value equal to the average of the maximum and minimum allowable supply voltage. The signal generator shall be adjusted such that the voltage input at the amplifier under test swings between maximum and minimum specified values. Then:

$$PS_{rr} = \frac{\Delta V_o}{A_d \Delta V_{cc}}$$

Where: ΔV_o = Change in output voltage (peak)

ΔV_{cc} = Change in supply voltage (peak)

A_d = Open loop gain

The frequency used shall be selected as specified in 3.2.1.

4. SUMMARY. The following details shall be specified in the applicable procurement document for specified values of C_1, C_2, R_1, and R_2.

(a) V_{cmi} at specified temperature(s).
(b) CM_{rr} at specified temperature(s), V_i and signal frequency.
(c) PS_{rr}, when applicable, at specified temperature(s).
(d) Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperature and at 25°C ambient.

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METHOD 4003 - Continued

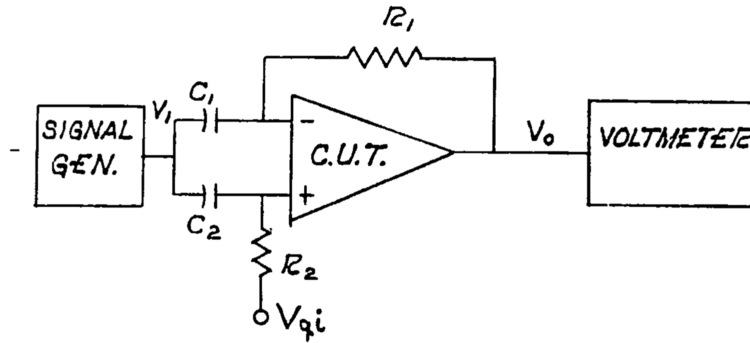

FIGURE 4003-1

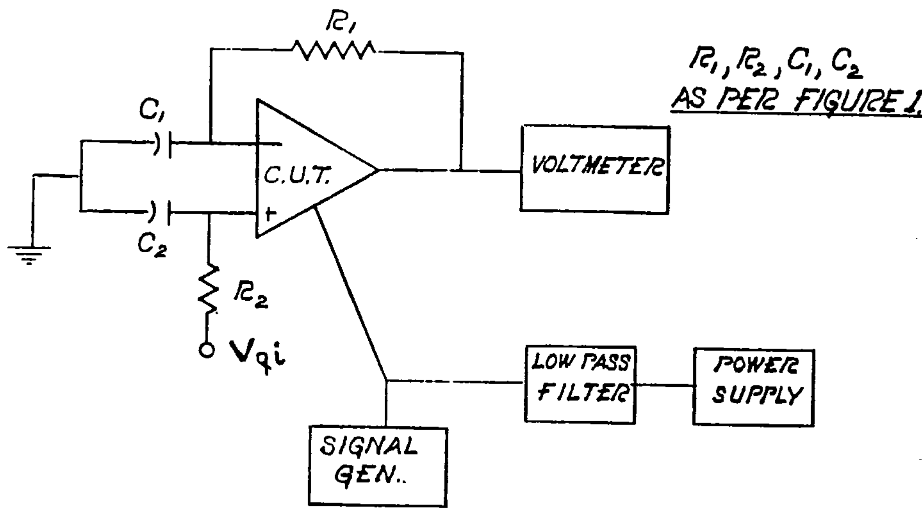

FIGURE 4003-2

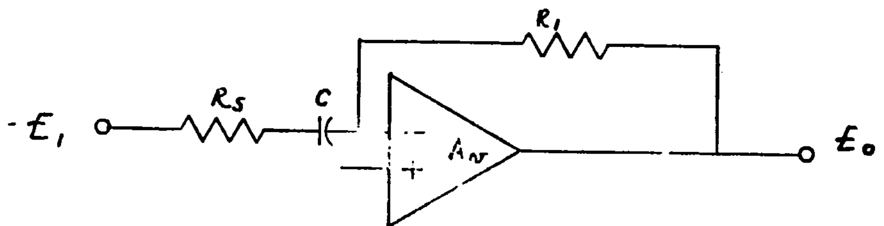

FIGURE 4003-3.

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METHOD 4004

OPEN LOOP PERFORMANCE

1. PURPOSE. The purpose of this test procedure is to measure gain, bandwidth, distortion, dynamic range, and input impedance. Gain, dynamic range and distortion are combined into a large signal test where the distortion measurement will indicate either lack of dynamic range or inherent distortion.'

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Maximum output voltage swing (V_{om}). The maximum output voltage swing is the maximum peak-to-peak output voltage which can be obtained without waveform clipping when the quiescent DC output voltage is set at a specified reference level.

1.1.2 Single ended input impedance (Z_{in}). The single ended input impedance is the ratio of the change in input voltage to the change in input current seen between either input and ground with the other input terminal AC grounded. In case of single input amplifiers it is the impedance between that terminal and ground. It is measured at the quiescent output DC level.

1.1.3 Differential input impedance (Z_{di}). The differential input impedance is the ratio of the change in input voltage to the change in input current seen between the two ungrounded input terminals of the amplifier at the quiescent output DC level.

1.1.4 Differential voltage gain (A_d). The differential voltage gain (open loop) is the ratio of the AC output voltage to the differential AC input voltage.

1.1.5 Single ended voltage gain (A_v). The single ended voltage gain (open loop) is the ratio of the AC output voltage to the single ended or differential AC input voltage. In the case of differential input amplifiers the input not connected to the signal source is at zero AC potential.

1.1.6 Bandwidth, open loop (BW_{ol}). The open loop bandwidth is the range of frequencies within which the open-loop voltage gain of the amplifier is not more than 3 db below the value of the midband open loop gain.

1.1.7 Distortion. The total ratio of the RMS sum of all harmonics to the total RMS voltage at the output for a pure sine wave input.

2. APPARATUS. The apparatus will consist of a signal generator, AC voltmeter, distortion analyzer, resistors, and capacitors.

2.1 Signal generator. This shall be a sine wave generator of low distortion which can cover the frequency range of the amplifier under test.

2.2 Voltmeter. The voltmeter shall be capable of measuring the amplifier AC output voltage without loading and shall have a frequency range that will cover the amplifier under test.

2.3 Distortion meter. The distortion analyzer or meter shall be useable over the passband of the amplifier. An alternate to the use of a distortion meter would be a suitable filter to reject the fundamental frequency while not attenuating the harmonics. The filter output can then be measured with the AC voltmeter and compared with the reading ahead of the filter.

2.4 Resistors and capacitors. Resistors shall be within 1 percent or better of the specified values with low inductance and capacitors shall be within 10 percent or better of the specified values with low dissipation factor. R_2 shall be equal to the minimum specified input impedance of the device under test.

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METHOD 4004 - Continued

3. PROCEDURE. The same test figure (figure 4004-1) shall be used for all of the tests. A differential input is shown, but if a single ended inverting amplifier is under test the components shown at the positive input terminal shall not be used. If a noninverting amplifier is under test is shall be necessary to either use fixed bias instead of the DC feedback or to use an inverting gain of one amplifier in the feedback path. For differential output devices, the measurements described in 3.1, 3.2, 3.3, and 3.4 below, as applicable, shall be repeated for the other output using the same test figure except that the measuring equipment shall be connected to the other output. Referring to the circuit of figure 4004-2, the transfer function is:

$$\frac{E_O}{E_1} = \frac{A_V}{1 + \frac{(A_V + 1)(R_S - jX_C)}{R_1}}$$

The error term which shall be maintained at 0.1 or less for a 10% maximum inherent error is:

$$\frac{(A_V + 1)(R_S - jX_C)}{R_1}$$

3.1 Open loop gain. For this test switch S is closed. The signal generator frequency shall be set to a specified value and V_1 brought up until V_2 is a specified reading on the voltmeter.

$$A_d = A_V = \frac{V_2}{V_1} \quad \frac{(R_3 + R_4)}{R_4}$$

3.2 Distortion. Under the conditions of 3.1 read the distortion on the distortion meter or the voltage at the output of the rejection filter if that is used.

3.3 Maximum output voltage swing. This is an implied measurement in that the tests of 3.1 and 3.2 will be performed with the value of V_2 at the maximum specified for the circuit. The distortion will be excessive if the circuit does not have sufficient dynamic range.

3.4 Bandwidth. Establish the amplitude of V_2 within the linear region of the device under test at a frequency specified for the measurement of A_d. Increase the frequency, while maintaining the amplitude of V_1 constant, until V_2 reduces to 0.707 of the original value (3 db down). This frequency shall be measured as the bandwidth for the device under test.

3.5 Input impedance. This will be specified as a minimum value and shall be measured by observing that the output voltage V_2 does not drop more than 6 db (2:1 in voltage) when the switch S is opened. This test shall be performed at the specified frequency with a specific amplitude of V_2 within the linear region. R_2 shall be given as the value of the minimum input impedance.

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METHOD 4004 - Continued

4. SUMMARY. The following details shall be specified in the applicable procurement document for specified values of R_1, R_2, and C:

(a) V_{om}, at specified temperature(s).
(b) Z_{in} (minimum), at specified temperature(s) and frequency.
(c) Z_{di}, where applicable, at specified temperature(s) and frequency.
(d) A_d, where applicable, at specified temperature(s) and frequency.
(e) A_v, at specified temperature(s) and frequency.
(f) BW_{o1}, at specified temperature(s).
(g) Distortion (%), at specified temperature(s).
(h) V_{qi}, when applicable, at specified temperature(s).
(i) Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperatures and at 25°C ambient.

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METHOD 4004 - Continued

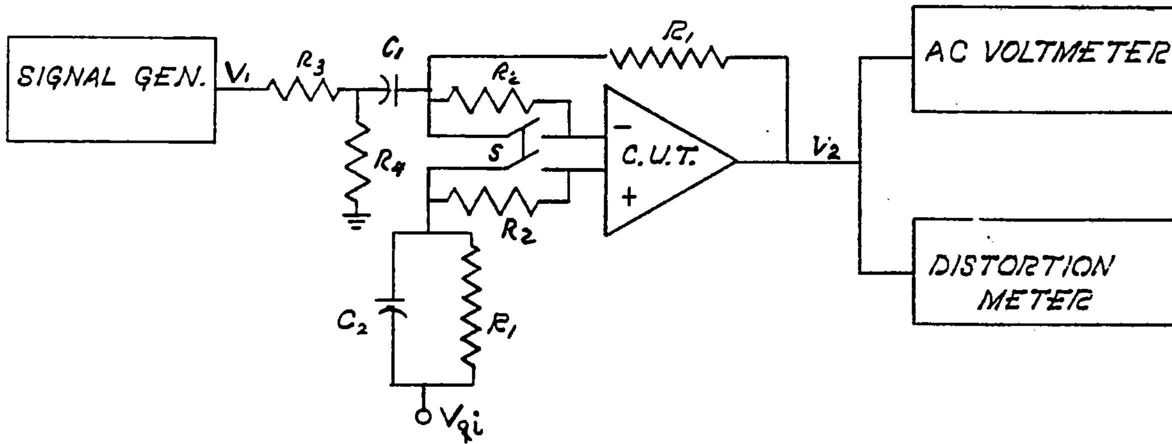

FIGURE 4004-1

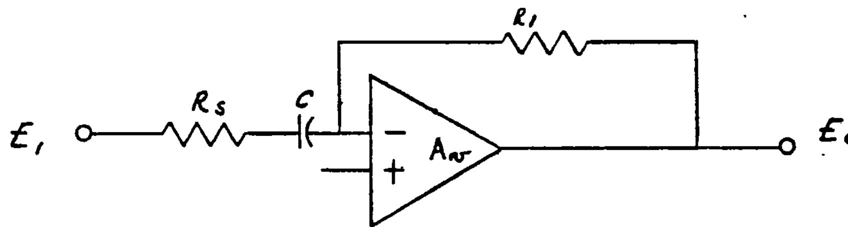

FIGURE 4004-2

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METHOD 4005

OUTPUT PERFORMANCE

1. PURPOSE. This method establishes the means for measuring the power dissipation and output impedance.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Output impedance (Z_o). The output impedance is the impedance between the output terminal and ground. It is measured at a specific quiescent DC output voltage and with no AC feedback around the amplifier.

1.1.2 Power dissipation (P_d). The power dissipation is the total power dissipated in the amplifier with the amplifier biased into its normal operating range and without any output load.

2. APPARATUS. The apparatus will consist of a signal generator, AC voltmeter, DC current meter, DC voltmeter, resistors and capacitors.

2.1 Signal generator. This shall be a sine wave generator which can cover the frequency range of the amplifier under test.

2.2 AC voltmeter. The AC voltmeter shall be capable of measuring the voltage without loading the circuit. For instance, its input impedance should be at least ten times the amplifier output impedance of the amplifier under test. The useful frequency range should be at least as high as that of the amplifier.

2.3 DC voltmeter. The DC voltmeter should have an input impedance at least ten times the output impedance of the amplifier under test. Accuracy should be such that it will not contribute to the acceptable error. For example, if the parameter to be measured has a tolerance of 10 millivolts, the voltmeter should be accurate to better than 1 millivolt.

2.4 DC current meter. This is used to measure the current from the power supplies and should cover the range required for the circuit under test.

2.5 Resistors and capacitors. These should be sufficiently stable to enable the test to be made. R_2 shall be within 1% or better of the specified value.

3. PROCEDURE. The test figure shown will be used for all three tests. R_1 should be no larger than the nominal input impedance nor less than a value which will load the amplifier ($100 \times Z_{out}$). $2\pi f R_1 C_1$ shall be at least $10A_d$ where A_d is the open loop gain and f is the test frequency. C_2 should be at least $\frac{10}{2\pi f R_2}$ and R_2 should be about equal to the nominal amplifier Z_o.

3.1 Power dissipation. For this test the signal generator is off. Measure the positive supply voltage and current V_{cc} and I_c and the negative supply voltage and current V_{EE} and I_E. The power dissipation $P_d = V_{cc} I_c + V_{EE} I_E$.

3.2 Output impedance. For this test the signal generator frequency is set to a specified value and the level is set to a specified V_2. V_o is read on the AC voltmeter. The output impedance is then equal to:

$$Z_o = \frac{V_o R_2}{V_2 - V_o}$$

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METHOD 4005 - Continued

An alternate measurement would be to make R_2 equal to the maximum acceptable value of Z_0 and require that V_0 be no greater than $V_2/2$. For differential output devices, this measurement shall be repeated for the other output using the same test figure except that the measuring equipment shall be connected to the other output.

4. SUMMARY. The following details shall be specified in the applicable procurement document for specified values of R_1, R_2, C_1, and C_2.

(a) Z_0 limits at the specified frequency.
(b) P_d maximum.
(c) V_2 where applicable.
(d) V_{qi} where applicable at the specified temperature(s).
(e) Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperature and at 25°C ambient.

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METHOD 4005 - Continued

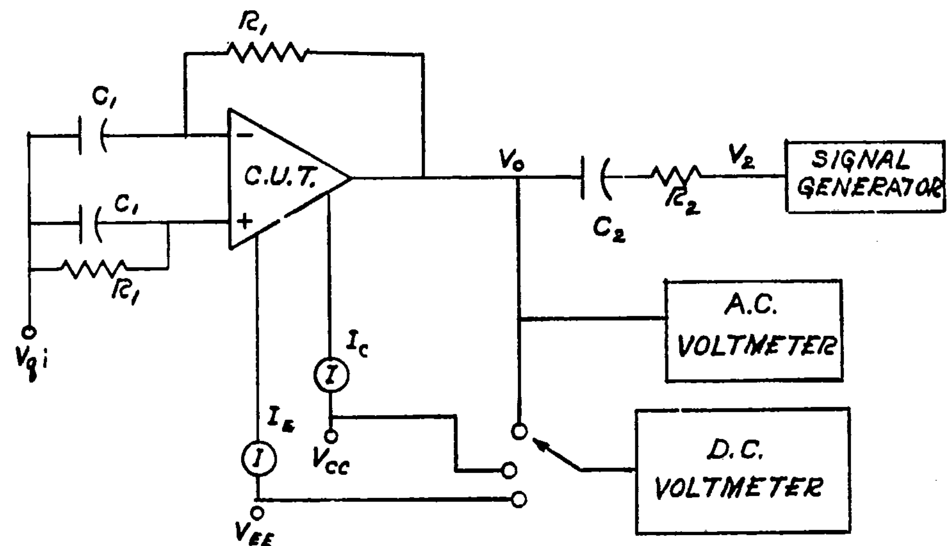

FIGURE 4005-1

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METHOD 4006

POWER GAIN AND NOISE FIGURE

1. PURPOSE. The purpose of this test procedure is to measure small signal power gain, and the noise figure of an amplifier.

1.1 Definition. The following definitions shall apply for the purpose of this test method.

1.1.1 Power gain (PG). The power gain is the ratio, expressed in dB, of the signal power developed at the output of the amplifier to the signal power applied to the input.

$$PG = 10 \log \frac{P_{OUT}}{P_{IN}}$$

1.1.2 Noise factor (F). The noise factor is the ratio of the signal-to-noise power ratio at the input to the signal-to-noise power ratio at the output.

$$F = \frac{\frac{P_{IN}}{N_{PIN}}}{\frac{P_{OUT}}{N_{POUT}}}$$

Where:
- P_{IN} = input signal power
- P_{OUT} = output signal power
- N_{PIN} = input noise power
- N_{POUT} = output noise power

1.1.3 Noise figure (NF). The noise figure (NF) is the noise factor (F) expressed in db.

$$NF = 10 \log F = 10 \log \left(\frac{P_{IN}/N_{PIN}}{P_{OUT}/N_{POUT}} \right)$$

The above expression for NF can be written in terms of voltage since the signal and its associated noise work into the same load.

$$NF = 20 \log \frac{\frac{V_{IN}}{N_{IN}}}{\frac{V_{OUT}}{N_{OUT}}} = 20 \log \frac{V_{IN}}{N_{IN}} - 20 \log \frac{V_{OUT}}{N_{OUT}}$$

Where:
- V_{IN} = signal voltage IN
- V_{OUT} = signal voltage OUT
- N_{IN} = noise voltage IN
- N_{OUT} = noise voltage OUT

2. APPARATUS. The apparatus will consist of a signal generator, AC voltmeter, resistors, capacitors, potentiometer, sweep generator, oscilloscope, peak detector, filter, and noise generator.

2.1 Signal generator. This shall be a sine wave generator of low distortion which can cover the frequency range of the amplifier under test. It shall have a calibrated attenuator, calibrated output level and a known output resistance (R_g).

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METHOD 4006 - Continued

2.2 AC voltmeter. The AC voltmeter shall be true RMS reading with a scale calibrated in db and shall be capable of measuring the amplifier AC output voltage without loading and shall have a frequency range that will cover the frequency range of amplifier under test.

2.3 Resistors, capacitors, and potentiometer. The resistors, capacitors, and potentiometer shall be stable over the required test temperature range and shall have values within 1 percent of the specified resistance and capacitance.

2.4 Sweep generator. The sweep generator must cover the range of the amplifier under test. It shall have an adjustable output level which is flat over the sweep range.

2.5 Oscilloscope. The oscilloscope shall have a frequency response wider than the circuit under test and shall be compatible with the sweep generator for synchronization.

2.6 Peak detector. The peak detector shall be linear over the range of output voltages without loading the circuit under test.

2.7 Filter. A filter capable of isolating the noise bandwidth (ΔF) shall be used. It should be specified in conjunction with the signal frequency of interest and shall present a load to the amplifier similar to its load in normal operation. The filter noise power bandwidth must be accurately known.

2.8 Noise generator. This shall be a temperature-limited diode noise generator with a calibrated source resistance (R_g) and an accurately calibrated output noise current meter.

3. PROCEDURE. The test figures show the connections for the various test conditions. The signal frequency, where applicable, shall be a specified value within the defined bandwidth of the amplifier.

3.1 Power gain. Figure 4006-1 is used for this test. Unless otherwise specified, R_2 shall be equal to the nominal output impedance of the device under test. If the input resistance (R_i) of the device under test is much greater than the source resistance (R_g), unless otherwise specified, a resistor (R) which makes $V_I = 1/2\ V_g$ should be added in series with R_g. The specified AC signal V_g at the specified frequency is applied to the inputs of the amplifier under test. V_I and V_L are recorded. Then:

$$PG(dB) = 10 \log \left[\frac{V_L^2}{V_1(V_g - V_1)} \times \frac{R_g}{R_2} \right]$$

If the series resistor (R) has been added, then:

$$PG(dB) = 10 \log \left[\frac{V_L^2}{V_1\ (V_g - V_1)} \times \frac{R_g'}{R_2} \right]$$

Where:

$$R_g' = R_g + R$$

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METHOD 4006 - Continued

3.2 Power gain (insertion method). If the input resistance (R_i) to the device under test is known, the power gain can be measured by this procedure. In figure 4006-2 with switch S in position 1, and the attenuator set to zero insertion loss, a reference level is established on the oscilloscope. The switch is then moved to position 2, switching in the circuit under test, and the attenuation increased until the output is brought to the previous reference level. The voltage insertion gain of the circuit under test equals the attenuator setting in dB. The power gain is then calculated from the following expression:

$$PG(dB) = (\text{Attenuator reading}) + 20 \log \left[\frac{R_i (R_g + R_2)}{R_2 (R_g + R_i)} \right]$$

Where: R_2 equals the nominal output impedance of the circuit under test.
R_g equals the source resistance.
R_i equals the input impedance of the circuit under test, unless otherwise specified.

The accuracy of this measurement is dependent upon the accuracy of the attenuator.

3.3 Noise figure. Figure 4006-3 is used for this test. The input noise voltage shall be calculated from the following expression:

$$N_{IN} = \sqrt{4KT\Delta f \pm R_g}$$

Where:
K = Boltzmann's constant (1.38×10^{-23} joules/°K)
T = Temperature (°K)
Δf = Noise bandwidth
R_g = Source resistance

The input signal level is then set to ten times (20 dB) N_{IN}. R_x is now adjusted so that the AC voltmeter reads 10 dB on some convenient scale. The input signal V_g is then reduced to zero and the reduction in dB on the output recorded. The noise figure NF is obtained by subtracting this drop in dB from 20 dB. The error in this measurement can be calculated from the following expression:

$$\text{Error (dB)} = 10 \log \left[\left(\frac{V_{OUT}}{N_{OUT}} \right)^2 + 1 \right] - 20 \log \frac{V_{OUT}}{N_{OUT}}$$

It should be noted that the error will always be in a direction to indicate a lower noise figure than the true noise figure.

3.4 Noise figure, alternate method. In this test a diode noise generator, as shown in figure 4006-4, is used to measure the noise figure. In this test, with switches S_1 and S_2 in position 1 and the source resistance (R_s) adjusted to a specified value, a reference voltage is read on the AC voltmeter. The switches S_1 and S_2 are then moved to position 2 and the diode source current (I) increased until the previous reference level is read on the AC voltmeter. Using the value of I and R_s the noise figure is determined for the following expression:

$$NF = 10 \log 20 IR_s$$

The accuracy of this technique is established by the accuracy of the 3 db pad and the current meter in the noise diode circuit.

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METHOD 4006 - Continued

3.5 Noise factor. The noise factor can be determined from the following expression:

$$NF = 10 \log F$$

In this expression NF is in dB and F is a numeric.

4. SUMMARY. The following details shall be specified in the applicable procurement document for specified values of R_2 and R_g:

(a) PG, at specified temperature(s), and frequency, and R_2.
(b) NF, at specified temperature(s), and frequency.
(c) F, at specified temperature(s), and frequency.
(d) Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperatures and at 25°C ambient.
(e) Noise bandwidth (Δf) (see 3.3).
(f) R_s (see 3.4).
(g) R and R_2, when applicable (see 3.1).

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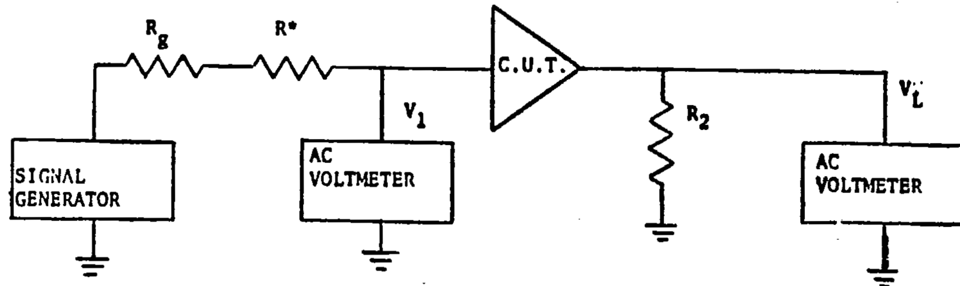
METHOD 4006 - Continued



* When required (see 3.1)

FIGURE 4006-1. Power gain test circuit.

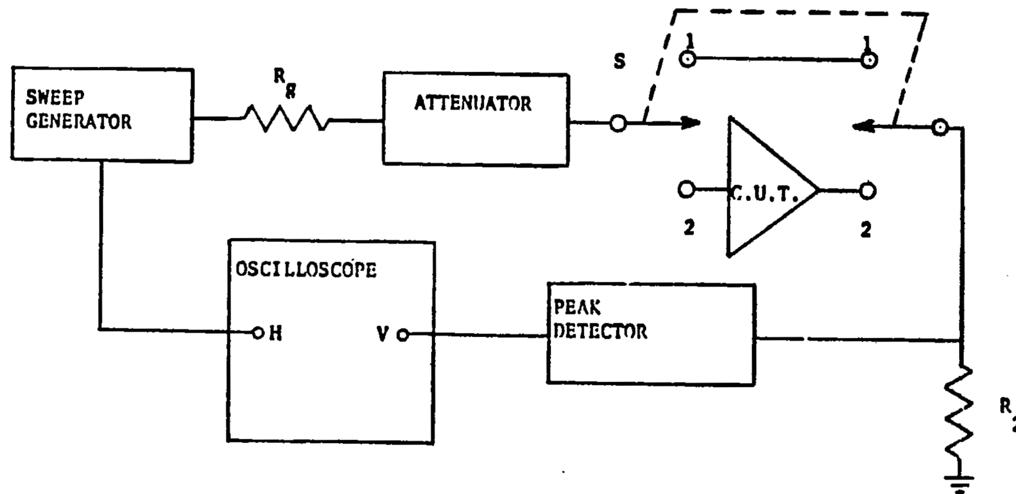


FIGURE 4006-2. Power gain test circuit (insertion method).

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METHOD 4007

AUTOMATIC GAIN CONTROL RANGE

1. PURPOSE. This method establishes the means for measuring the automatic gain control range of a linear amplifier.

1.1 Definitions. The following definition shall apply for the purpose of this test method.

1.1.1 Automatic gain control range (AGC). The AGC range is the total change in voltage gain which may be achieved by application of a specified range of DC voltages to the AGC input terminal of the device.

$$AGC = 20 \log \frac{A_{V\,max}}{A_{V\,min}}$$

2. APPARATUS. The apparatus shall consist of a sweep generator, voltage source, resistors, capacitors, an AC voltmeter, and a distortion analyzer.

2.1 Sweep generator. The sweep generator must cover the frequency range of the amplifier under test. It shall have an adjustable output level which is flat over the sweep range. It shall be capable of single frequency operation.

2.2 Voltage source. The voltage source shall be capable of supplying the specified AGC voltages to the test circuit. The voltage source shall be free of noise or ripple at its outputs.

2.3 Capacitors and resistors. The capacitors and resistors shall be within 1% or better of the specified values and stable over the test temperature range.

2.4 AC voltmeter. The AC voltmeter shall be capable of measuring the amplifier output voltage without loading and shall have a frequency range that will cover the amplifier under test.

2.5 Distortion analyzer. The distortion analyzer or meter shall be usable over the passband of the amplifier and shall not load the amplifier.

3. PROCEDURE. The test circuit shown in figure 4007-1 shall be used for this test. R_L and C_1 shall be selected to properly load and decouple the circuit, respectively. The AGC voltage is set for maximum gain. The input signal is applied (constant frequency) and increased until the output exhibits maximum allowable distortion. The generator is swept over the prescribed range and the bandwidth noted.

The AGC voltage is varied over the specified range and the reduction in gain is measured. The above measurements are repeated and the bandwidth and signal handling capability recorded.

4. SUMMARY. The following details shall be specified in the applicable procurement document for specified values of C_1 and R_L.

(a) AGC range.
(b) Test frequency range.
(c) Increase in bandwidth over the AGC range.
(d) Maximum reduction in output impedance, where applicable.
(e) Minimum reduction in input signal capability, where applicable.
(f) Any other variations when applicable, such as power variation, overloading, limitations as to linearity of gain response versus AGC voltage, etc.
(g) Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified ambient operating temperature and at 25°C ambient.

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METHOD 4007 - Continued

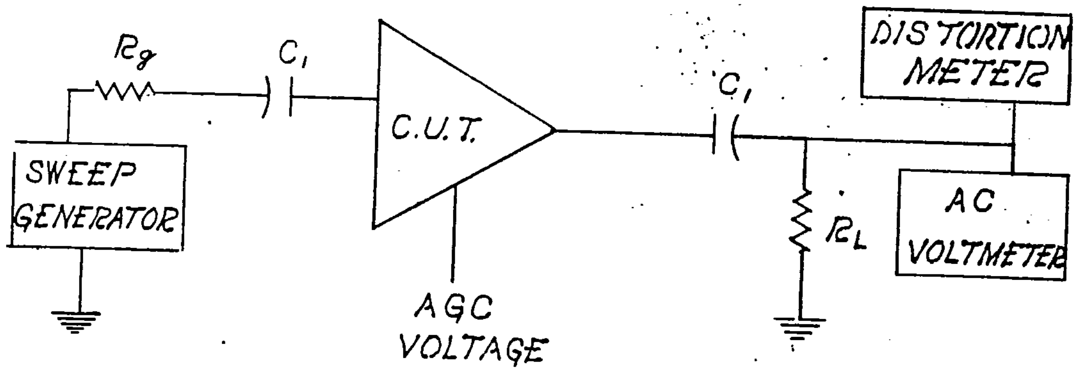

FIGURE 4007-1. AGC test circuit.

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This tentative test method has been prepared by USAF/RADC-17. It is optional for use by all activities.

METHOD T5001

PARAMETER MEAN VALUE CONTROL

1. PURPOSE. The purpose of this method is to define a technique for assuring a conformance to a maximum or minimum mean of a parameter measured in any test method listed in section 3000 and 4000 of this standard. This method is not intended for general application to procurements where it is important only to assure that device parameters are between specified limits. It is intended for use only where it is necessary to control the average or mean value for a given parameter throughout a lot or shipment of devices. When this method is employed, it is expected that the specified group of devices tested will be packaged for shipment as a group together with the required data. It is also expected that some provisions will be required for special marking of devices subjected to this method to identify that they have met the selection criteria involved and that they are therefore not directly interchangeable with identical devices which have not been controlled or selected in this manner.

2. APPARATUS. For distribution control, it is desirable for the measuring equipment to have data logging capability in addition to the capabilities listed in section 3000 and 4000. The data shall be recorded and analyzed to compute the average value of a group of microelectronic devices. The size of the group shall be specified in the applicable procurement document.

3. PROCEDURE. Microelectronic devices shall be separated into groups. Each group will be tested as per the specified test method. The reading from each device will be recorded. When all devices in the group have been tested, the recorded data shall be averaged (or the mean value computed) and compared against a maximum or minimum limit specified in the applicable procurement document.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Absolute maximum and minimum limits.
(b) Maximum or minimum limits on the average or mean.
(c) Group size.
(d) Requirements for data logging, special marking and special provisions for group packaging and shipment, where applicable.

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This tentative test method has been prepared by USAF/RADC-17. It is optional for use by all activities.

METHOD T5002

PARAMETER DISTRIBUTION CONTROL

1. PURPOSE. The purpose of this method is to define a technique for assuring a normal distribution for any test method listed in section 3000 or 4000 of this standard. This method is not intended for general application to procurements where it is important only to assure that device parameters are between specified limits. It is intended for use only where it is necessary to control the distribution of parameter values within the specified group. When this method is employed, it is expected that the specified group of devices tested will be packaged for shipment as a group together with the required data. It is also expected that some provisions will be required for special marking of devices subjected to this method to identify that they have met the selection criteria involved and that they are therefore not directly interchangeable with identical devices which have not been controlled or selected in this manner.

2. APPARATUS. For distribution control, it is desirable for the measuring equipment, in addition to the capabilities listed in section 3000 and 4000, to have the capability of rejecting and counting the devices above or below the specified extreme limits, and to also separate and count the devices that fall above or below the one sigma limits. If the equipment does not have this capability, the units shall be read to the specified parameter conditions and the data recorded. Identification of units to the data shall also be required. Data analysis and unit separation shall be hand performed in the case where automatic equipment is not used.

3. PROCEDURE. Microelectronic devices shall be separated into groups. Each group will be tested, as per the specific method for the maximum and minimum limits specified in the applicable procurement document. All failures will be removed from the original group. The remaining units will be tested for the following: Not less than 12% but not greater than 18% of units tested will fall below the mean - 1σ limit. Not greater than 18% but not less than 12% of units tested will fall above the mean $+1\sigma$ limit.

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Absolute maximum and minimum limits.
(b) Mean value.
(c) $+1\sigma$ and -1σ value.
(d) Group size.
(e) Requirements for data logging, special markings and special provisions for packaging and shipment, were applicable.

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This tentative test method has been prepared by USAF/RADC-17. It is optional for use by all activities.

METHOD T5003

FAILURE ANALYSIS PROCEDURES FOR MICROCIRCUITS

1. PURPOSE. Failure analysis is a post mortem examination of failed devices employing, as required, electrical measurements and many of the advanced analytical techniques of physics, metallurgy, and chemistry in order to verify the reported failure and identify the mode or mechanism of failure as applicable. The failure analysis procedure (as indicated by test condition letter) shall be sufficient to yield adequate conclusions, for determination of cause or relevancy of failure or for initiation of corrective action in production processing, device design, test or application to eliminate the cause or prevent recurrence of the failure mode or mechanism reported.

1.1 Data requirements. When required by the applicable procurement document the failure analyst shall receive, with the failed part, the following information:

(a) Test conditions: This shall include the type of test or application, the in-service time (when available), temperature and other stress conditions under which the device failed.
(b) System conditions: This shall include the exact location of failure in the equipment, date, test and/or inspection at which defect was first noted, any unusual environmental conditions and all related system anomalies noted at time of removal of the failed unit. The equipment symptoms shall also be recorded.
(c) General device information: This shall include part type numbers and serial numbers (when applicable), date code and other identifying information, and size of production or inspection lot (when applicable).

2. APPARATUS. The apparatus required for failure analysis includes electrical test equipment capable of complete electrical characterization of the device types being analyzed, micromanipulators capable of point-to-point probing on the surface of device dies or substrates, as required, and microscopes capable of making the observations at the magnifications indicated in the detailed procedures for the specified test condition. In addition, special analytical equipment for bright field, dark field and phase contrast microscopy, metalographic sectioning and angle lapping are required for the test condition C. Special analytical equipment for test condition D are as detailed in the procedure and shall be available only as required for each specific device analysis at that level. Apparatus for X-ray radiography, hermeticity test and other specific test methods shall be as detailed in the referenced method. Cleaning agents, chemicals for etching, staining, oxide or metalization removal shall be available as required.

3. PROCEDURE. Failure analysis shall be performed in accordance with the specified test condition letter (see 4).

3.1 Test condition A. Failure verification. This represents a minimal diagnosis, comprised of the electrical verification of the failure including external and internal photographic recording of the suspected mode or mechanism of failure. The following steps (see 3.1.1 thru 3.1.5) shall be performed in the sequence indicated and the results included in the failure analysis report. The sequence may be modified or additional tests performed when justified by an analysis of the results of previous steps in the sequence.

3.1.1 External examination. This shall include an optical examination at a magnification of 30X minimum of:

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METHOD T5003 - Continued

(a) The condition of the leads, plating, soldered or welded regions.
(b) Condition of external package material, seals, marking and other features as warranted.

Photographic records shall be made at suitable magnification of any unusual features.

3.1.2 Electrical verification procedures. This shall include the measurement of all electrical parameters in the applicable procurement document.

3.1.3 Additional electrical tests. These shall be performed specifically for the determination of opens and shorts:

(a) Threshold test. Determine the forward characteristic obtained for each pin to substrate and compare to the device schematic and structure. Excessive forward voltage drop may indicate an open or an abnormally high resistance current path.
(b) Case isolation. (For metal packages or those with metal lids or headers only.) Apply a voltage between the package and the external leads. Current flow determines the presence of shorts-to-case.
(c) As an alternative to (a) and (b) above, suitable electrical tests may be made to determine that no opens, shorts, or abnormal characteristics exist between pairs of pins, pins and die or substract, or pins and device package.

3.1.4 Internal examination. The lid of the failed device shall be carefully removed and an optical examination made of the internal device construction at a minimum magnification of 30X. A color photograph, at suitable magnification to show sufficient detail, shall be taken of any anomalous regions which may be related to the device failure.

3.1.5 Information obtainable. The following is a partial list of failure modes and mechanisms which may be identified using test condition A:

(a) Overstress conditions resulting from device abuse, transients or inadequate power supply regulation, evidenced as open or shorted leads, and other metallization problems, such as flashover between contacts within the circuit.
(b) Excessive leakage currents indicating degraded junctions.
(c) Resistance changes.
(d) Degradation of time response or frequency dependent parameters.
(e) Opens and shorted leads and/or metallization land areas.
(f) Undercut metals.
(g) Intermetallic formation.
(h) Poor bond placement and lead dress.
(i) Thin metal at oxide steps.
(j) Migration of metal.
(k) Oxide contamination - discoloration.
(l) Oxide defects, cracks, pinholes.
(m) Mask misregistration.
(n) Reactions at metal/semiconductor contact areas.
(o) Degradation of lead at lead frame.
(p) Shorts through the oxide or dielectric.
(q) Missing or peeling metals.
(r) Corroded metals within package.
(s) Cracked die or substrate.

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3.2 Test condition B. This is a more extensive procedure which supplements test condition A with x-ray radiography, seal testing, additional electrical measurements, package cleaning, vacuum baking, and probing procedures to aid in confirmation of suspected modes and mechanisms. The following steps shall be performed in the sequence indicated and the results included in the failure analysis report. The sequence may be modified or additional tests performed when justified by an analysis of the results of previous steps in the sequence.

3.2.1 External examination. This shall include an optional examination at a magnification of 30X minimum of:

(a) The conditions of leads, platings, soldered or welded regions.
(b) Condition of external package material, seals, markings and other features as warranted.

Photographic records shall be taken at suitable magnification of any unusual features.

3.2.2 Electrical verification procedures. This shall include the measurement of all electrical parameters in the applicable procurement document.

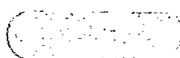
3.2.3 Additional electrical tests. In addition to the threshold and case isolation tests, this section provides for curve tracer pin to pin measurements and other nonstandard measurements which allow electrical characterization of significant physical properties.

(a) Threshold test. Determine the forward characteristic obtained for each pin to substrate and compare to the device schematic and structure. Excessive forward voltage drop may indicate an open or abnormally high resistance in the current path.
(b) Case isolation. (For metal packages or those with metal lids or headers only.) Applying a voltage between the package and the external leads. Current flow determines the presence of shorts-to-case.
(c) Pin-to-pin two and three terminal electrical measurements, utilizing a transistor curve tracer, electrometer, pico ammeter, capacitance bridge, and oscilloscope, as required, shall be performed and results recorded for lead combinations involving the defective portion of the microcircuit. Gain, transfer, input vs. output, forward and reverse junction characteristics, shall be observed and interpreted. Resulting characteristics may be compared to those obtained from a good unit, and differences interpreted for their relation to the device failure.

3.2.4 X-ray radiography. A film record is required of the failed device taken normal to the top surface of the device, and where applicable, additional views shall be recorded. This shall be performed when open or shorted leads, or the presence of foreign material inside the device package are indicated from electrical verification of failure or there is evidence of excessive temperature connected with the device failures.

3.2.5 Fine and gross seal testing. This shall be performed in accordance with Method 1014 of this standard.

3.2.6 External package cleaning. When there is evidence of contamination on the package exterior, the device shall be immersed in standard degreasing agents followed by boiling deionized water. After drying in clean nitrogen, critical parameters in the applicable procurement document shall be remeasured in accordance with paragraph 3.2.1 above.



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3.2.7 Internal examination. The lid of the failed device shall be carefully removed and an optical examination made of the internal device construction, at a minimum magnification of 30X. A color photograph, at suitable magnification to show sufficient detail, shall be taken of any anomalous regions which may be related to the device failure. Where there is evidence of foreign material inside the device package, it shall removed using a stream of dry compressed inert gas or appropriate solvents. The relationship of the foreign material to device failure (if any) shall be noted and if possible, the nature of the material shall be determined.

3.2.8 Electrical verification procedures. Critical parameters of the individual specification shall be remeasured and recorded.

3.2.9 Vacuum bake. This shall be performed at the suggested conditions 10^{-5} torr, 150°C to 250°C for two hours noting any change in leakage current, as a result of baking, using a micromicroammeter.

3.2.10 Electrical verification procedures. Critical parameters of the individual specification shall be remeasured and recorded.

3.2.11 Multipoint probe. A multipoint probe shall be used as applicable to probe active regions of the device to further localize the cause of failure. A curve tracer shall be used to measure resistors, the presence of localized shorts and opens, breakdown voltages, and transistor gain parameters. A micromicroammeter shall be used for measuring leakage currents, and where applicable, a capacitance bridge shall be employed for the determination of other junction properties. It may be necessary to open metallization stripes to isolate components.

3.2.12 Information obtainable. The procedures of test condition B can result in the following information in addition to that outlined in 3.1.5:

(a) Hermeticity problems.
(b) Radiographically determined defects such as poor wire dress, loose bonds, open bonds, voids in die or substrate mount, presence of foreign materials.
(c) Further definition of failed device region.
(d) Stability of surface parameters.
(e) Quality of junctions, diffusions and elements.

3.3 Test condition C. In this procedure additional metallographic analysis techniques are provided to supplement the analysis accomplished in test condition B, and shall be performed after completion of the full procedure of test condition B. In test condition C, one of the procedures (see paragraphs 3.3.1, 3.3.2 and 3.3.3) shall be selected as appropriate and the steps shall be followed in the sequences indicated. The sequence may be modified or additional tests performed when justified by the analysis of the results of previous steps in the sequence.

3.3.1 Total device cross section. This procedure shall be used where there are indications of defects in the package, die or substrate, bonds, seals or structural elements. The following steps shall be performed:

(a) Mount the device in the appropriate orientation for cross sectioning procedures.
(b) Section to reveal desired feature(s) and stain where applicable.
(c) Employ bright field, dark field, or polarized light photomicrography at suitable magnification.
(d) Make photographic record of defective regions or features pertinent to the mode or mechanism of failure.

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METHOD T5003 - Continued

3.3.2 Oxide defect analysis. This procedure shall be used where there are indication of oxide (or other dielectric) structural anomalies or contamination within or under the oxide or where it is necessary to determine the specific location and structure of such defects. The following steps shall be performed:

(a) Remove bonds to die or substrate and remove metallized interconnection layer(s).
(b) Observe the oxide using interferometric and/or phase contrast photomicrography at suitable magnification and make appropriate photographic record.
(c) Observe and probe semiconductor contact (window or cut) areas as applicable, recording appropriate electrical characteristics.
(d) Mount the die or substrate in the appropriate orientation for sectioning (angle or cross) procedures, cut or lap to reveal desired features and stain where applicable.
(e) Make photographic record at suitable magnification.

3.3.3 Diffusion defect analysis. This procedure shall be used where there are indications of diffusion imperfections, diffusion of contact metal into the semiconductor, structural defects in the semiconductor or anomalies in junction geometries. The following steps shall be performed:

(a) Remove bonds to die or substrate and remove metallized interconnection layer(s).
(b) Remove oxide or other dielectric passivation layer.
(c) Probe contact regions recording appropriate electrical characteristics.
(d) Stain surface to delineate junctions.
(e) Mount the die or substrate in the appropriate orientation for angle lap or sectioning, angle or cross.
(f) Cut or lap as required to expose significant features and stain junctions (may involve successive lap and stain operations to approach specific defect).
(g) Make photographic record at suitable magnification of significant features and record pertinent electrical probing results.

3.3.4 Information obtainable. Failure analysis in accordance with test condition C provides additional capability for detecting or defining the following types of defects:

(a) Oxide or dielectric imperfections
(b) Oxide or dielectric thicknesses
(c) Diffusion imperfections
(d) Junction geometries
(e) Intermetallic phase formation
(f) Voids at the bond/metallization interface
(g) Diffusion of contact metal into the semiconductor or substrate
(h) Migration of metals across, through or under the oxide or dielectric
(i) Voids in die or substrate mount

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METHOD T5003 - Continued

3.4 Optional measurements. The purpose of failure analysis is to obtain sufficient information to initiate corrective action in device design, production or test. It may be necessary to obtain more detailed information than can be acquired in test conditions A, B or C on the nature of contaminants or phases observed, concentrations, dimensions of submicroscopic features, etc. The selection and use of a number of less conventional analytical techniques by highly qualified personnel can provide this more extensive or fundamental knowledge of the precise chemical, physical or electrical mechanisms of failure. The decision as to which techniques are appropriate and the point in the analytical sequence of test conditions A, B, or C at which they should be employed is contingent on the nature of information desired and previous results obtained from the specified analytical procedures, and must be left to the discretion of the analyst. Any of the following techniques may therefore be introduced into a failure analysis sequence at the appropriate point provided precautions are taken to avoid destruction of the evidence of failure which may be observed in subsequent procedures. Where multiple samples of the same type of device or failure exist, it shall be permissible to subdivide the quantity of devices and employ destructive techniques in parallel with the specified test condition provided all samples have been exposed to electrical verification tests and internal examination (see 3.1.1 through 3.1.3 and 3.2.1 through 3.2.5) prior to any of the optional measurements. When any of these optional measurements are employed, they shall be listed in the failure analysis report including the details of the method applied, conditions of test and results.

(a) Residual gas analysis. When device surface contamination is indicated as a possible cause of failure, the lid of an unopened device shall be punctured and the internal gaseous ambient analyzed for the type and concentration of volatile products. This information then supplements electrical leakage current measurements and hermeticity tests.

(b) Talysurf surface topography measurement. A mechanical determination of surface topography variations can be made using a talysurf instrument. This records the vertical motion of a stylus moved across the surface of the device. This information can be used to quantitatively determine oxide, dielectric or metal thicknesses.

(c) Photoscanning. A device, with leads and interconnections intact, after being opened, can be scanned with a small diameter beam of light which generates photovoltages in active p-n junctions. This generated photovoltage which is dependent on many physical junction properties indicates the presence of surface channels and/or inversion layers, caused by contamination on, in or under the passivating oxide layer. It is also possible to locate certain regions of enhanced high field multiplication, mask misregistration, imperfect diffusions, as well as other device imperfections involving junction properties.

(d) Infrared scanning. An IR detector, sampling infrared radiation from various points of the surface of an operating microcircuit can detect the location of hot spots and other thermal abnormalities.

(e) Electron beam microanalysis. An electron beam microanalysis can be used for x-ray spectrochemical analysis of micron sized volumes of material. Several other device structural properties are determinable through detection and display of backscattered primary electrons and secondary electrons. The instrument is most generally used for:

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METHOD T5003 - Continued

(1) determination of products of solid state reactions, such as diffusion, precipitation and intermetallic formation.
(2) analysis of micron sized defects such as oxide pin-holes, metallization grain structure.
(3) determination of surface potential variations using secondary electron scanning microscopy. The small size of the electron beam coupled with the properties of secondary electrons result in the ability to examine physical defects with much higher resolution and depth of field than light microscopy.

(f) Electron microscopy. An examination at extremely high magnification of the structure of failed metallization and bulk materials is best accomplished using electron microscopy.

(g) Special test structures. Often the amount of reacted material on a failed circuit is too small to allow definitive determination of chemical and structural properties. In addition, it is often necessary to reproduce the failure in a controlled experimental manner for verification of the mechanism of failure. Special test structures may be fabricated with variations in geometry and materials permitting study of the mechanism without extraneous influences. This is most advantageous when information is desired concerning the basic failure mechanism(s).

4. SUMMARY. The following details must be specified in the applicable procurement document:

(a) Test condition letter (see 3) for test conditions A, B, or C and where applicable, optional measurements (see 3.4), identifying the specific procedures to be applied and details as to their optional application.
(b) Any special measurements not described in the applicable test condition.
(c) Requirements for data recording and reporting including instructions as to disposition of original data, photographs, radiographs, etc.
(d) Physical and electrical specifications and limits for the device being analyzed.

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METHOD T5004

SCREENING PROCEDURES

1. PURPOSE. This method establishes screening procedures for total lot screening of microelectronics to assist in achieving levels of quality and reliability commensurate with the intended application. In recognition of the fact that the level of screening has a direct impact on the cost of the product as well as its quality and reliability, three standard levels of screening are provided to coincide with three device classes defined in terms of the technical and economic criticality of the application. Since it is not possible to prescribe an absolute level of quality or reliability which would result from a particular screening level or to make a precise value judgement on the cost of a failure in an anticipated application, three levels have been arbitrarily chosen. The method provides flexibility in the choice of conditions and stress levels to allow the screens to be further tailored to a particular source, product or application based on user experience. The user is cautioned to collect experience data so that a legitimate value judgement can be made with regard to specification of screening levels. Selection of a level better than that required for the specific product and application will, of course, result in unnecessary expense and a level less than that required will result in an unwarranted risk that reliability and other requirements will not be met. In the absence of specific experience data, the Class B screening level is recommended for military applications. Guidance in selecting screening levels or predicting the anticipated reliability for integrated circuits may be obtained from RADC TR-67-108, Vol II (AD 821640), "RADC Reliability Notebook".

1.1 Definitions. For the purpose of this test method, the following definitions shall apply:

(a) Class "A" - Devices intended for use where maintenance and replacement are extremely difficult or impossible, and reliability is imperative.

(b) Class "B" - Devices intended for use where maintenance and replacement can be performed, but are difficult and expensive, and where reliability is imperative.

(c) Class "C" - Devices intended for use where maintenance and replacement can be readily accomplished and down time is not a critical factor.

2. APPARATUS. Suitable electrical measurement equipments necessary to determine compliance with applicable procurement documents and other apparatus as required in the referenced test methods.

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3.0 PROCEDURE

3.1 Screening procedures for monolithic and multichip microcircuits. Screening shall be conducted as described in 3.1.1 through 3.1.15 and in the sequence shown, unless otherwise specified (see 4.0).

SCREEN	CLASS "A"		CLASS "B"		CLASS "C"	
	METHOD	SAMPLE	METHOD	SAMPLE	METHOD	SAMPLE
3.1.1 Internal visual (Precap)	2010, test condition A	100%	2010, test condition A	100%	2010, test condition B	100%
3.1.2 Stabilization bake	1008 48 hrs. min. (See paragraph 3.3 and 3.4.1)	100%	1008 48 hrs. min. (See paragraph 3.3 and 3.4.1)	100%	1008 48 hrs. min. (See paragraph 3.3 and 3.4.1)	100%
3.1.3 Thermal shock	1011 (See paragraph 3.3)	100%		---		---
3.1.4 Temperature cycling	1010 (See paragraph 3.3)	100%	1010 (See paragraph 3.3 and 3.4.2)	100%	1010 (See paragraph 3.3 and 3.4.2)	100%
3.1.5 Mechanical shock	2002, test condition F one shock pulse in Y_1 plane only <u>or</u> five shock pulses at condition B in Y1 plane	100%		---		---
3.1.6 Centrifuge	2001, Test condition E Y_1 plane, then Y_2 plane	100%	2001, test condition E Y_1 plane	100%	2001, Test condition D (min.) Y_1 plane only	100%
3.1.7 Hermeticity	1014		1014		1014	
a. Fine	a. Test condition A	100%	a. Test condition A	100%	a. Test condition A	100%
b. Gross 1. Transparent packages	b-1 Test condition C or D	100%	b-1 Test condition C or D	100%	b-1 Test condition C or D	100%
2. All other package types	b-2 Test condition C	100%	b-2 Test condition C	100%	b-2 Test condition C	100%
3.1.8 Critical electrical parameters	Per applicable procurement document (see paragraph 3.5.1)	100%		---		---
3.1.9 Burn-in test	1015 168 hrs @ 125°C min.	100%	1015 168 hrs @ 125°C	100%		---
3.1.10 Critical electrical parameters	Per applicable procurement document (see paragraph 3.5.1)	100%		---		---
3.1.11 Reverse bias burn-in (see para 3.4.3)	1015, test condition A or C 72 hrs @ 150°C min.	100%		---		---

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SCREEN	CLASS "A"		CLASS "B"		CLASS "C"	
	METHOD	SAMPLE	METHOD	SAMPLE	METHOD	SAMPLE
3.1.12 Final electrical test	Per applicable procurement document (See paragraph 3.5.2)		Per applicable procurement document (See paragraph 3.5.2)		Per applicable procurement document (See paragraph 3.5.2)	
a. DC parameters						
1. 25° C		100%		100%		100%
2. Maximum and minimum rated operating temp.		100%		---		---
b. AC parameters 25°C		100%		100%		100%
c. Functional test (see para 3.5.3) 25° C		100%		100%		---
d. Switching parameters 25° C		100%		---		---
3.1.13 Radiographic	2012	100%		---		---
3.1.14 Lot qualification	T5005	Per applicable document	T5005	Per applicable document	T5005	Per applicable document
3.1.15 External visual	2009	100%	2009	100%	2009	100%

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METHOD T5004 - Continued

3.2 Screening procedure for film hybrid microcircuits. Screening shall be conducted as specified in 3.1.1 through 3.1.15 above, except that the following changes shall apply:

(a) 3.1.1 Internal visual. Delete test condition A and replace with test condition C.
(b) 3.1.2 Stabilization bake. Delete time and replace with value as specified in the applicable procurement document.
(c) 3.1.3 Thermal shock. Test condition as specified in the applicable procurement document.
(d) 3.1.4 Temperature cycling. Test condition as specified in the applicable procurement document.
(e) 3.1.5 Mechanical shock. Delete test condition F and replace with value as specified in the applicable procurement document.
(f) 3.1.6 Centrifuge. Delete test conditions D and E and replace with value as specified in the applicable procurement document.

3.3 Temperature exposure. The temperature extremes of exposure for non-operating screens or tests shall be the maximum possible for the metallurgical system utilized without causing intermetallic formation or other undesirable interactions. The following are the recommended temperature extremes of exposure for specific metallization systems.

Metallurgical System	Temperature High	Temperature Low
Aluminum/Aluminum	200° C	-65° C
Gold/Aluminum	150° C	-65° C
Gold/Gold	300° C	-65° C

Where it is determined that exposure at -195° C is not detrimental to the device or package, -195° C is recommended as the low temperature extreme.

3.4 Substitution of tests, methods and sequence.

3.4.1 Stabilization bake. Gold-gold metallurgical system shall be subjected to stabilization bake in accordance with paragraph 3.1.2 immediately prior to performing internal visual, paragraph 3.1.1. For metallurgical systems other than gold/gold the stabilization bake may be conducted either after sealing or immediately prior to sealing of the devices. The high temperatures of exposure specified in paragraph 3.3 shall be the minimum stabilization bake temperatures for the indicated metallurgical systems. It shall also be permissable with metallurgical systems other than gold/gold to divide the total minimum stabilization bake time between pre-seal and post-seal bakes, so long as the total bake time equals or exceeds 48 hours and the post-seal bake time equals or exceeds 40 hours.

3.4.2 Temperature cycling. Paragraph 3.1.4, temperature cycling for class B and class C devices may be replaced with thermal shock, method 1011 in accordance with paragraph 3.1.3.

3.4.3 Burn-in. When test condition A is selected for the burn-in in condition of paragraph 3.1.9, the reverse bias burn-in requirement of paragraph 3.1.11 may be accomplished by continuing the burn-in of paragraph 3.1.9 for the additional 72 hours at the increased temperature, and the measurement of critical electrical parameters required in paragraph 3.1.10 may be accomplished as part of the final electrical test of paragraph 3.1.12.

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3.5 Electrical measurements

3.5.1 Critical electrical parameters. Electrical testing shall be performed to remove defective devices prior to conducting burn-in screening. This test need not include all specified device parameters, but shall include those measurements that are necessary to remove all electrically defective devices. When delta parameter measurements are required, they shall be specified in the applicable procurement document and shall be included as critical electrical measurements. When delta calculations are to be performed the procedures for device traceability shall be specified in the applicable procurement document.

3.5.2 Final electrical measurements. Final electrical testing of all device classes shall insure that each parameter specified in the applicable procurement document satisfies the specified values, limits, conditions and criteria.

3.5.3 Functional test(s). Functional test(s) shall be conducted only on digital circuits and shall consist of measurement of the relationship between inputs and outputs contained in the truth table(s). Measurements and sequence of test shall be specified in the applicable procurement document.

3.6 Data reporting. When required by the applicable procurement document data reporting shall be in accordance with the general requirements of paragraph 4.3.5 of this standard.

3.7 Failure analysis. When required by the applicable procurement document failure analysis of devices rejected during any test in the screening sequence of 3.0 above shall be accomplished in accordance with method T5003 of this standard. Requirements for such analysis should in general be limited to sufficient examination of devices to establish primary modes or mechanisms of failure and provide needed corrective action information.

3.8 Defective devices. All devices which fail to comply with the requirements of any screen or of the applicable procurement document shall be removed from the lot. Once rejected and verified as a device failure, no device may be retested for acceptance.

4.0 SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Procedure paragraph of method T5004, (see 3.1 and 3.2) and device class (see 1.1 and 3).
(b) Sequence of test, sample size and test method where not specified or if other than specified (see 3).
(c) Test condition, limit, cycles, temperature, axis, etc., where not specified, or if other than specified (see 3).
(d) Critical electrical parameters (see 3.1.8).
(e) Burn-in test condition (see 3.1.9).
(f) Delta parameter measurements including procedures for device traceability where applicable (see 3.5.1).
(g) Final electrical measurements (see 3.1.12).
(h) Temperature, (G) level, time and/or cycles as applicable in the following screens:
    (1) Stabilization bake (see 3.1.2 and 3.2b).
    (2) Thermal shock (see 3.1.3 and 3.2c).
    (3) Thermal cycling (see 3.1.4 and 3.2d).
    (4) Mechanical shock (see 3.2e).
    (5) Centrifuge (see 3.2f).
(i) Requirements for data recording and reporting, where applicable (see 3.6).
(j) Requirements for failure analysis (see 3.7).

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METHOD T5005

LOT QUALIFICATION INSPECTION

1. PURPOSE. This method establishes lot qualification inspection or lot acceptance procedures for microelectronics to assure that the lot quality conforms with the requirements of the applicable procurement document. In general, it is intended that the device class to which lot qualification inspection is conducted would be the same device class to which screening procedures (per method T5004) are conducted. However, it is permissible for lot qualification inspection requirements to be specified at a higher quality level (in no case shall a lower level be permitted) to reduce the potential percent-defective. It is also permissible to specify tightened inspection criteria for individual subgroups where experience indicates justifiable concern for specific quality problems.

1.1 Definitions. For the purpose of this test method, the following definitions shall apply:

(a) Class "A" - Devices intended for use where maintenance and replacement are extremely difficult or impossible, and reliability is imperative.
(b) Class "B" - Devices intended for use where maintenance and replacement can be performed, but are difficult and expensive, and where reliability is imperative.
(c) Class "C" - Devices intended for use where maintenance and replacement can be readily accomplished and down time is not a critical factor.
(d) LTPD series - The lot tolerance percent defective (LTPD) series is defined as the following decreasing series of LTPD or lambda (λ) values:

50, 30, 20, 15, 10, 7, 5, 3, 2, 1.5, 1.0, 0.7, 0.5, 0.3, 0.2, 0.15, 0.1.

(e) Tightened inspection - Tightened inspection is defined as inspection performed using the next LTPD or lambda value in the LTPD series lower than that specified.
(f) Acceptance number (c) - The acceptance number is defined as an integral number associated with the selected sample size which determines the maximum number of defectives permitted for that sample size.
(g) Rejection number (r) - Rejection number is defined as one plus the acceptance number.
(h) Minimum rejection number (MRN) - The minimum rejection number is defined as the minimum number of defectives that must be observed before the lot can be rejected.
(i) Production lot - A production lot shall consist of devices of a single type (part) number manufactured on the same production line(s) through final seal by means of the same production technique, materials, controls and design. Where a production lot identification is terminated upon completion of wafer or substrate processing or at any later point prior to device sealing, it shall be permissible to process more than a single device type (part) number in a single production lot provided all devices types are structurally similar and provided traceability is maintained by assembling devices into inspection lots as defined herein at the point where production lot identification is terminated.

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METHOD T5005 - Continued

(j) Inspection lot - An inspection lot is a collection of microelectronic devices submitted at one time for inspection to determine compliance with the acceptance criteria of the applicable procurement document. Each inspection lot shall consist of microelectronic devices of a single type or, when allowed by the applicable document, may consist of a collection of structurally similar device types. Inspection lot identification shall be maintained from the time the lot is assembled to the time it is accepted or given a final rejection.

2. APPARATUS. Suitable electrical measurement equipment necessary to determine compliance with the requirements of the applicable procurement document and other apparatus as required in the referenced test methods.

3. PROCEDURE. The procedure contained in 3.1 and 3.2 shall apply to lots containing 200 or more devices and the procedures contained in 3.8 shall apply to lots containing less than 200 devices.

3.1 Lot qualification procedures for monolithic and multichip microcircuits. Lot quality conformance inspections shall be conducted as described in the electrical subgroups 1 through 4 and environmental subgroups 1 through 10 in the sequence shown, unless otherwise specified (see 4.0).

TABLE I

ELECTRICAL TEST

	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
Subgroup 1 D.C. parameters Maximum and minimum rated operating temperature (See paragraph 3.5 of method T5004)	-	5	10
Subgroup 2 A.C. parameters Maximum and minimum rated operating temperature (See paragraph 3.5 of method T5004)	5	5	10
Subgroup 3 Functional (see paragraph 3)			
a. 25° C	-	-	20
b. Maximum and minimum rated operating temperature (See paragraph 3.5 of method T5004)	5	10	20
Subgroup 4 Switching parameter			
a. 25° C	-	10	20
b. Maximum and minimum rated operating temperature (See paragraph 3.5 of method T5004)	5	10	20

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METHOD T5005 - Continued

TABLE II

ENVIRONMENTAL TEST

TEST	METHOD	CONDITIONS	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
Subgroup 1					
Visual and mechanical and marking permanency	2008	Test condition B	10	15	20
Physical dimensions		Test condition A			
Subgroup 2					
Solderability	2003		10	15	20
Subgroup 3					
Thermal shock	1011	(See paragraph 3.3 of method T5004)	10	15	20
Temperature cycling	1010	Test condition C			
Moisture resistance	1004				
Critical electrical parameters		As specified in the applicable procurement document (See paragraph 3.5 of method T5004)			
Subgroup 4					
Mechanical shock	2002	Test condition B	10	15	20
Vibration fatigue	2005	Test condition A			
Vibration, variable frequency	2007	Test condition A			
Constant acceleration	2001	Test condition E			
Critical electrical parameters		As specified in the applicable procurement document (See paragraph 3.5 of method T5004)			
Subgroup 5					
Lead fatigue	2004	Test condition B_2	10	15	20
Hermeticity test	1014				
a. Fine		a. Test condition A			
b. Gross					
1. Transparent package		b.1. Test condition C or D			
2. All other package types		b.2. Test condition C			
Subgroup 6					
Salt atmosphere	1009	Test condition A	10	15	20
Subgroup 7					
High temperature storage	1008	$150 {}^{+50}_{-25}$ °C storage, 1000 hrs minimum	7	15	20
Critical electrical parameters		As specified in the applicable procurement document (See paragraph 3.5 of method T5004)			

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METHOD T5005 - Continued

TABLE II

ENVIRONMENTAL TEST - Continued

TEST	METHOD	CONDITIONS	CLASS A LTPD	CLASS B LTPD	CLASS C LTPD
Subgroup 8 Operating life testing Critical electrical parameters	1005	Test condition to be specified in the applicable procurement document (1000 hrs minimum) As specified in the applicable procurement document (See paragraph 3.5 of method T5004)	7	10	15
Subgroup 9 Steady state reverse bias Critical electrical parameters	1015	Test condition A, 72 hrs @ 150°C As specified in the applicable procurement document (See paragraph 3.5 of method T5004)	7	10	--
Subgroup 10 Bond strength (see paragraph 3.7) a. Thermocompression b. Ultrasonic or wedge	2011	a. Test condition B, C or D b. Test condition C or D	10 devices Not greater than 1% defective (See paragraph 3.7)	10 devices Not greater than 1% defective (See paragraph 3.7)	--

3.2 Lot qualification procedures for film hybrid microcircuits. Lot quality conformance inspection shall be conducted as described in tables I and II of paragraph 3.1 above except that the following changes shall apply:

(a) Environmental subgroup 3, thermal shock - Delete test condition F and replace with conditions as specified in the applicable procurement document.
(b) Environmental subgroup 3, temperature cycling - Delete test condition C and replace with test as specified in the applicable procurement document.
(c) Environmental subgroup 4, constant acceleration - Delete test condition E and replace with value as specified in the applicable procurement document.

3.3 Acceptance procedure. The acceptance number (c) and/or the minimum reject number (MRN) shall be specified in the applicable procurement document and the procedure for lot acceptance shall be as described below unless otherwise specified (see 4).

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METHOD T5005 - Continued

TABLE III. LTPD Sampling plans. 1/ 2/ 3/

Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent-defective equal to the specified LTPD will not be accepted (single sample).

Max. Percent Defective (LTPD) or λ	50	30	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2	0.15	0.1
Acceptance Number (c) (r = c + 1)	Minimum Sample Sizes (For device-hours required for life test, multiply by 1000)																
0	5 (1.03)	8 (0.64)	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)	1152 (0.005)	1534 (0.003)	2303 (0.002)
1	8 (4.4)	13 (2.7)	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.045)	1296 (0.027)	1946 (0.018)	2592 (0.013)	3891 (0.009)
2	11 (7.4)	18 (4.5)	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.47)	266 (0.31)	354 (0.23)	533 (0.15)	759 (0.11)	1065 (0.080)	1773 (0.045)	2662 (0.031)	3547 (0.022)	5323 (0.015)
3	13 (10.5)	22 (6.2)	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)	3341 (0.041)	4452 (0.031)	6681 (0.018)
4	16 (12.3)	27 (7.3)	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)	3997 (0.049)	5327 (0.037)	7994 (0.025)
5	19 (13.8)	31 (8.4)	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)	4638 (0.056)	6181 (0.042)	9275 (0.028)
6	21 (15.6)	35 (9.4)	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)	5267 (0.062)	7019 (0.047)	10533 (0.031)
7	24 (16.6)	39 (10.2)	57 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)	5886 (0.067)	7845 (0.051)	11771 (0.034)
8	26 (18.1)	43 (10.9)	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)	6498 (0.072)	8660 (0.054)	12995 (0.036)
9	28 (19.4)	47 (11.5)	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)	7103 (0.077)	9468 (0.057)	14206 (0.038)
10	31 (19.9)	51 (12.1)	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)	7704 (0.080)	10268 (0.060)	15407 (0.040)
11	33 (21.0)	54 (12.8)	83 (8.3)	111 (6.2)	166 (4.2)	238 (2.9)	332 (2.1)	555 (1.2)	832 (0.83)	1109 (0.62)	1664 (0.42)	2378 (0.29)	3323 (0.21)	5546 (0.12)	8319 (0.083)	11092 (0.062)	16638 (0.042)
12	36 (21.4)	59 (13.0)	89 (8.6)	119 (6.5)	178 (4.3)	254 (3.0)	356 (2.2)	594 (1.3)	890 (0.86)	1187 (0.65)	1781 (0.43)	2544 (0.3)	3562 (0.22)	5936 (0.13)	8904 (0.086)	11872 (0.065)	17808 (0.043)
13	38 (22.3)	63 (13.4)	95 (8.9)	126 (6.7)	190 (4.5)	271 (3.1)	379 (2.26)	632 (1.3)	948 (0.89)	1264 (0.67)	1896 (0.44)	2709 (0.31)	3793 (0.22)	6321 (0.134)	9482 (0.089)	12643 (0.067)	18964 (0.045)
14	40 (23.1)	67 (13.8)	101 (9.2)	134 (6.9)	201 (4.6)	288 (3.2)	403 (2.3)	672 (1.4)	1007 (0.92)	1343 (0.69)	2015 (0.46)	2878 (0.32)	4029 (0.23)	6716 (0.138)	10073 (0.092)	13431 (0.069)	20146 (0.046)
15	43 (23.3)	71 (14.1)	107 (9.4)	142 (7.1)	213 (4.7)	305 (3.3)	426 (2.36)	711 (1.41)	1066 (0.94)	1422 (0.71)	2133 (0.47)	3046 (0.33)	4265 (0.235)	7108 (0.141)	10662 (0.094)	14216 (0.070)	21324 (0.047)
16	45 (24.1)	74 (14.6)	112 (9.7)	150 (7.2)	225 (4.8)	321 (3.37)	450 (2.41)	750 (1.44)	1124 (0.96)	1499 (0.72)	2249 (0.48)	3212 (0.337)	4497 (0.241)	7496 (0.144)	11244 (0.096)	14992 (0.072)	22487 (0.048)
17	47 (24.7)	79 (14.7)	118 (9.86)	158 (7.36)	236 (4.93)	338 (3.44)	473 (2.46)	788 (1.48)	1182 (0.98)	1576 (0.74)	2364 (0.49)	3377 (0.344)	4728 (0.246)	7880 (0.148)	11819 (0.098)	15759 (0.074)	23639 (0.049)
18	50 (24.9)	83 (15.0)	124 (10.0)	165 (7.54)	248 (5.02)	354 (3.51)	496 (2.51)	826 (1.51)	1239 (1.0)	1652 (0.75)	2478 (0.50)	3540 (0.351)	4956 (0.251)	8260 (0.151)	12390 (0.100)	16520 (0.075)	24780 (0.050)
19	52 (25.5)	86 (15.4)	130 (10.2)	173 (7.76)	259 (5.12)	370 (3.58)	518 (2.56)	864 (1.53)	1296 (1.02)	1728 (0.77)	2591 (0.52)	3702 (0.358)	5183 (0.256)	8638 (0.153)	12957 (0.102)	17276 (0.077)	25914 (0.051)
20	54 (26.1)	90 (15.6)	135 (10.4)	180 (7.82)	271 (5.19)	386 (3.65)	541 (2.60)	902 (1.56)	1353 (1.04)	1803 (0.78)	2705 (0.52)	3864 (0.364)	5410 (0.260)	9017 (0.156)	13526 (0.104)	18034 (0.078)	27051 (0.052)
25	65 (27.0)	109 (16.1)	163 (10.8)	217 (8.08)	326 (5.38)	466 (3.76)	652 (2.69)	1086 (1.61)	1629 (1.08)	2173 (0.807)	3259 (0.538)	4656 (0.376)	6518 (0.269)	10863 (0.161)	16295 (0.108)	21726 (0.081)	32589 (0.054)

1/ Sample sizes are based upon the Poisson exponential binomial limit.

2/ The minimum quality (approximate AQL) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.

3/ The life test failure rate Lambda (λ) shall be defined as the LTPD per 1000 hours.

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METHOD T5005 - Continued

3.3.1 Acceptance procedure if minimum rejection numbers (MRN) are not specified. For the first sampling, an acceptance number shall be chosen and the associated number of sample devices for the specified LTPD selected and tested. If the observed number of defectives from the first sample is less than or equal to the preselected acceptance number, the lot shall be accepted. If the observed number of defectives exceeds the preselected acceptance number, an additional sample may be chosen such that the total sample complies with paragraph 3.3.4.

3.3.2 Acceptance procedure if minimum rejection numbers (MRN) are specified. The first sample shall be selected in accordance with 3.3.1 using an acceptance number less than the specified MRN. If the observed number of defectives from the first sample is equal to or less than the preselected acceptance number for the sample size, the lot shall be accepted. If the observed number of defectives on the first sample equals or exceeds the MRN, the lot shall not be accepted. If the observed number of defectives exceeds the preselected acceptance number but is less than the specified MRN, an additional sample may be chosen. The additional sample shall be in accordance with 3.3.4 and shall be equal to the difference between the first sample and the sample associated with an acceptance number which is one less than the specified MRN. The lot shall be accepted if the sum of the defectives from both samples is less than the specified MRN.

3.3.3 Sample selection. Samples shall be randomly selected from the assembled inspection lot after specified screening requirements of method T5004 have been satisfactorily completed. In table II, subgroup 1, "visual and mechanical", subgroup 2, "solderability", subgroup 5, "lead fatigue and hermeticity" and subgroup 6, "salt atmosphere", devices may be used that are electrical rejects, when end point measurements are not required. In table I "electrical", a single sample may be used for all subgroup testing. In table II "environmental", devices used in subgroup 3, "thermal and moisture resistance" may be used in subgroup 4, "mechanical".

3.3.4 Additional sample. The supplier may add an additional quantity to the initial sample, but this may be done only once for any subgroup and the added samples shall be subjected to all the tests within the subgroup. The total sample size (initial and added samples) shall be determined by a new acceptance number from table III. If an MRN is specified, the size of the additional sample shall comply with the 3.3.2.

3.4 Disposition of samples. Add devices used in table I "electrical" subgroup tests that comply with the requirements contained in the applicable procurement document may be returned to the lot. In table II all tests with the exception of subgroup 7, "high temperature storage", subgroup 8, "operational life" and subgroup 9, "steady state reverse bias" shall be considered destructive and all units subjected to these tests shall be properly identified and removed from the lot. Devices that have been subjected to subgroup 7, "high temperature storage", subgroup 8, "operational life" or subgroup 9, "steady state reverse bias" may be returned to the lot upon completion of testing provided:

(a) The devices are packaged separately and clearly marked life test samples.
(b) All devices are measured and they meet all electrical characteristics as specified in the applicable procurement document.

3.5 Resubmission of failed lots for qualification. Unless otherwise specified in the applicable procurement document when a lot fails any subgroup qualification requirements of 3.1 and 3.2, it may be resubmitted a maximum of one time for qualification of that particular subgroup using tightened inspection criteria (see 1.1e) provided an analysis is performed to determine the failure mechanism for each reject device and it is determined that the failures are due to:

(a) Testing error resulting in electrical damage to devices:
(b) A defect that can be effectively removed by rescreening the entire lot;
(c) Random type defects which do not reflect poor basic device design or poor workmanship.

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METHOD T5005 - Continued

When two or more subgroup tests are failed in table I testing or three or more subgroup tests are failed in table II testing, that lot shall not be resubmitted for qualification. In all instances where analysis of the devices from lots that fail qualification indicate that the failure mechanism is due to poor workmanship, a basic design fault, or nonscreenable defects, the lot shall not be resubmitted for qualification.

3.6 Life test lot rejection procedure.

3.6.1 Procedure to be used if number of observed failures exceeds the acceptance number. In the event that the number of failures observed in table II testing of subgroup 7,"high temperature storage" and subgroup 8, "operational life" exceeds the acceptance number, the supplier shall choose one of the following options: (1) discontinue the life test, screen or rework and submit per paragraph 3.5, (2) add additional samples in accordance with 3.3.4. Only one option shall be used for a given submission, and this option shall be used only once.

3.6.2 Catastrophic failures. An catastrophic failure as defined in the applicable procurement document during table II testing of subgroup 7, "high temperature storage", subgroup 8, "operational life", subgroup 9, "steady state reverse bias" shall fail the lot. If such a failure should occur, the lot may be resubmitted in accordance with 3.5.

3.7 Bond strength. Devices selected for bond strength testing shall have their lids carefully removed. All internal leads shall be tested and their strength shall comply with the minimum strength specified in the applicable procurement document.

3.8 Small lot qualification. Lot qualification testing for lots containing less than 200 devices shall be conducted as directed below unless otherwise specified (see 4).

3.8.1 Class "A" and Class "B" lot qualification shall be achieved by subjecting the entire lot to and operating life test for a minimum of 240 hours conducted at 125° C and at the maximum operational rating of the device in accordance with method 1005. Intermediate measurements at the 168 hour point need not be made. The test condition shall be specified in the applicable procurement document. At the completion of 240 hours of testing all devices shall be measured to determine that they comply with all electrical characteristics and end point measurements as specified in the applicable procurement document. When delta parameter measurements and calculations are required they shall be specified in the applicable procurement document.

3.8.2 Class "C" lot qualification shall be achieved by subjecting the entire lot to an operating life test for a minimum of 240 hours at the maximum rated operating temperature of the device in accordance with procedures of method 1005. The test condition shall be specified in the applicable procurement document. At the completion of 240 hours of test all devices shall be measured to determine that they comply with all electrical characteristics as specified in the applicable procurement document.

3.8.3 Small lot qualification criteria. The criteria for qualification shall be that the observed percent defective at the completion of 1000 hours operating life testing shall not exceed 2% of the total devices tested for class A devices, 3% for class B devices and 6% for class C devices. Resubmission of failed lots shall not be permitted

3.9 Data reporting. When required by the applicable procurement document the following data shall be provided for each lot submitted for qualification:

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(a) Results of each subgroup test.
(b) Number of devices rejected.
(c) Failure mechanism of each rejected device.
(d) Number of additional samples added, when applicable.
(e) Resubmitted lots, identification and history.

4. SUMMARY. The following details shall be specified in the applicable procurement document:

(a) Device class (see 1.1 and 3) and procedure paragraph of method 5005 (see 3.1, 3.2, and 3.8).
(b) Sequence of test, sample size, test method and test condition where not specified or if other than specified.
(c) Test temperature where not specified or when other than 25° C.
(d) Test condition cycles, temperature, axis, etc., where not specified or if other than specified (see 3.2).
(e) Acceptance procedure (see 3.3), and LTPD if other than specified (see 3).
(f) Final electrical parameters.
(g) Critical electrical parameters.
(h) Requirements for failure analysis (see 3.5).
(i) Bond strength (see 3.7).
(j) Requirements for data recording and reporting where applicable (see 3.9).
(k) Limits on maximum lot size or frequency of requalification where applicable.
(l) Restrictions on resubmission of failed lots (see 3.5), where applicable.

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This tentative test method has been prepared by USAF/RADC-17. It is optional for use by all activities.

METHOD T5006

LIMIT TESTING

1.0 PURPOSE. This method provided means for establishing or evaluating the maximum capabilities of microelectronic devices, including such capabilities as absolute maximum ratings (from which safe design limits may be derived), maximum stresses which may be applied in screening or testing without causing degradation, and sensitivity to particular screening or testing without causing degradation, and sensitivity to particular screening or testing stresses and the associated modes or mechanisms of failure. Since this is a relatively expensive and time consuming procedure, it is not intended for general application to all device procurements. It should however be extremely useful in evaluating the capabilities of new device types or devices which have experienced significant modifications in design, materials or processes which might be expected to alter their stress tolerance or primary modes and mechanisms of failure. It should also be useful in providing information vital to quality and reliability assurance in high reliability programs or in procurement extending over significant periods of time where test results can be used to provide corrective action in device design, processing or testing.

1.1 Destructive testing. All limit testing accomplished in accordance with this method is considered destructive and devices shall be removed from their respective lot.

1.2 Parameter measurements. Electrical measurement shall be performed to remove defective devices after each stress step unless otherwise specified herein or in the applicable procurement document. These measurements need not include all device parameters, but shall include sufficient measurements to detect all electrically defective devices. When delta parameter measurements are required they shall be specified in the applicable procurement document.

2.0 APPARATUS. The apparatus for this test shall include equipment specified in the referenced test methods as applicable and electrical measurement equipment necessary to determine device performance.

3.0 PROCEDURE. Limit testing shall be conducted in accordance with the procedure contained in 3.1 and 3.2 using samples sizes as designated in table I.

TABLE I

Limit Test	Sample size
Thermal evaluation	5
Extended thermal shock	10
Step-stress mechanical shock	10
Step-stress constant acceleration	10
Step-stress operational life	10
Constant high stress operational life	10
Step-stress storage life	10
Total devices	65

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3.1 Test condition A. Procedure for monolithic and multichip microcircuits. Limit testing shall be conducted as described in 3.1.1 through 3.1.7 in the sequence shown, unless otherwise specified (see 4.0). Failure analysis of all devices failing limit tests shall be performed in accordance with method T5003, test condition B, unless otherwise specified in the applicable procurement document. Limit testing may be discontinued prior to completing the test when 50% of the test sample has failed that specific test.

3.1.1 Thermal evaluation. This test shall be performed in accordance with method 1012, test condition B. With maximum power applied, the complete temperature gradient of the active chip area shall be recorded. This data shall be analyzed to determine that no areas of abnormally high operating temperatures are present as a result of improper design or processing. The thermal resistance at the maximum operating temperature of the device shall be determined using test condition C of method 1012.

3.1.2 Extended thermal shock. The purpose of this testing is to establish the resistance of the device to thermal fatigue effects. The device shall be subjected to a minimum of 100 cycles of thermal shock, in accordance with method 1011. This test shall be conducted in the following sequence:

Step	Cycles	Test condition
1	15	C
2	15	D
3	70	F

Parameter measurements (see 1.2) shall be made at the completion of 15, 30, 40, 70, and 100 cycles, and the number of failures after each of these cycles shall be recorded.

3.1.2.1 Temperature cycling. When specified in the applicable procurement document, temperature cycling method 1010 may be substituted for the thermal shock test in 3.1.2. This test shall be conducted in the following sequence:

Step	Cycles	Test condition
1	20	B
2	20	C
3	20	D

Parameter measurements (see 1.2) shall be made at the completion of each step, and the number of failures for each of these steps shall be recorded.

3.1.3 Step-Stress mechanical shock. The purpose of this test is to establish the mechanical integrity of the device. The device shall be subjected to mechanical shock in accordance with method 2002 and the following step-stress sequence:

Step	Test condition	Plane	No. of shocks
1	B	Y_1	5
2	C	Y_1	5
3	E	Y_1	5
4	F	Y_1	5
5	G	Y_1	5

Electrical parameter measurements (see 1.2) shall be made after each step, and the number of failures incurred at each step shall be recorded.

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3.1.4 Step-stress constant acceleration. The purpose of this testing is to establish the mechanical integrity of the device. The device shall be subjected to a constant acceleration in accordance with method 2001 and the following step-stress sequence:

Step	Test condition	Plane
1	E	Y_2, X_1, Z_1, Y_1
2	F	Y_2, X_1, Z_1, Y_1
3	G	Y_2, X_1, Z_1, Y_1
4	H	Y_2, X_1, Z_1, Y_1

Electrical parameter measurements (see 1.2) shall be made after each plane, and the number of failures incurred shall be recorded.

3.1.5 Step-stress operational life. The purpose of this test is to establish the operational stress levels that will accelerate predominant failure mechanisms so that meaningful failures can be generated in a relatively short period of time. The results of the testing will also be utilized to evaluate the safety factors built into the device, to establish the safe constant operational stress conditions, and to improve through corrective action(s) the reliability of the device. Electrical parameter measurements shall be made after each stress level and the number of failures incurred in each step shall be recorded.

3.1.6 Constant high-stress operational life. The purpose of this test is to induce meaningful operational failures in a relatively short period of time and to compare the results of this testing with the results obtained from the step-stress operational life. The stress level to be applied and intervals for intermediate electrical measurements shall be determined on the basis of the results obtained in the step-stress tests (see 3.1.5). Electrical parameter measurements shall be made after each specified time interval and the number of failures shall be recorded.

3.1.7 Step-stress storage life. The purpose of this test is to establish the storage stress levels that will accelerate predominant failure mechanisms so that meaningful failures can be generated in a relatively short period of time. The storage temperatures and the step duration shall be established prior to initiation of testing. The results of the testing will be utilized to evaluate the maximum limits of device resistance to failure at high temperature. Electrical parameter measurements shall be made after each stress level and the number of failures incurred at each level shall be recorded.

3.2 Test condition B. Procedure for film and hybrid microcircuits. Limit test shall be conducted in accordance with table I and as described in 3.1.1 through 3.1.7 except that the specified test condition may be changed. When test condition or stress levels are changed, they shall be established prior to the initiation of test. Failure analysis of all devices failing limit tests shall be performed in accordance with method T5003, test condition B, unless otherwise specified in the applicable procurement document. Unless otherwise specified in the applicable procurement document, limit testing in any test may bediscontinued after 50% of test sample has failed that specific test.

3.3 Test plan. When required by the applicable procurement document, the specific procedures for conducting limit testing shall be submitted as a "Limit Test Plan"for approval by the procuring activity prior to the initiation of testing. This plan shall include the following as a minimum:

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METHOD T5006 - Continued

a. Activity responsible for performing the test.
b. Device types to be subjected to limit testing and criteria for their selection.
c. Failure criteria including electrical parameters to be measured.
d. Testing schedule.
e. Description of testing equipment.
f. Test condition if other than specified.
g. Data recording and reporting formats.
h. Data analysis procedures.

4.0 SUMMARY. The following details shall be specified in the applicable procurement document:

a. Test condition letter (see 3.1 and 3.2).
b. Test sequence and sample quantities if other than specified (see 3.1 and 3.2).
c. Failure analysis procedures and test condition, if other than specified (see 3.1 and 3.2).
d. For test condition B, the test conditions and stress levels, where applicable (see 3.2).
e. Percent failure for test termination, if other than specified (see 3.1 and 3.2).
f. Requirements for Limit Test Plan and data reporting (see 3.3).

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